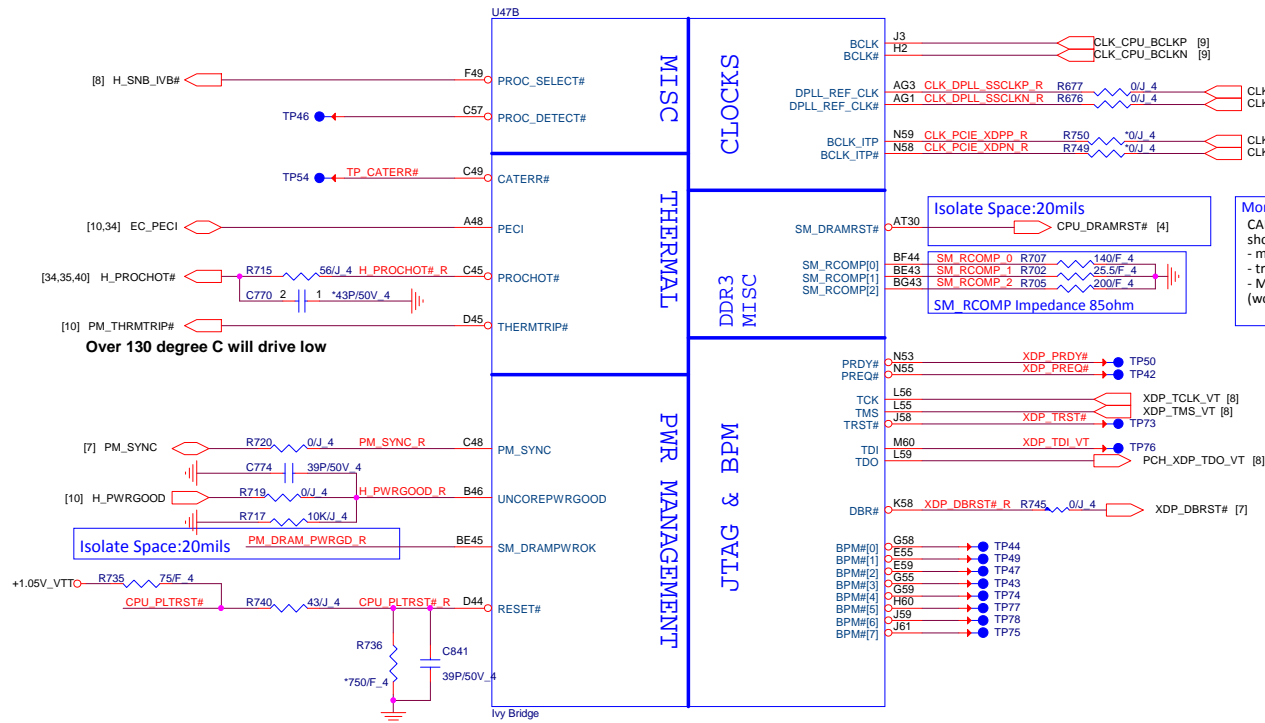


DG 1.0 :
The recommended AC cap value is changed to 220nF for compatibility with
PCIe Gen3 on future platforms.
For Gen2 only designs, it is acceptable to continue to use the 100nF capacitor.



| | | |
|-------|---|---------------|
| Size | Document Number | Rev |
| | Ivy Bridge 1/5 (HOST & PCIE) | 1A |
| Date: | Monday, January 07, 2013 | Sheet 2 of 46 |

Ivy Bridge Processor (CLK,MISC,JTAG) (CPU)



If motherboard only supports external graphics or if it supports Processor Graphics but without xDP:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK on Processor to VCCP through 1K +/- 5% resistor.

Memory Down Layout notes
CAD NOTE: All DDR, COMP signals should be routed such that :-
- max length = 500 mils
- trace width = 15mils and
- MB trace impedance < 68 mohms (worst case resistance)

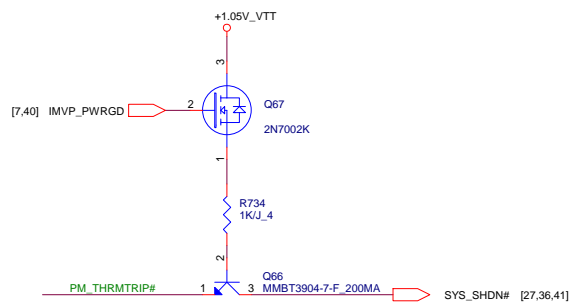
Layout Notes: Place near to XDP connector
05/15 : PCH_XDP_TDO_VT already pull high
+3V_S5 on PCH side

Option for Prochot# function
68 ohm for unused, 62 ohm for used

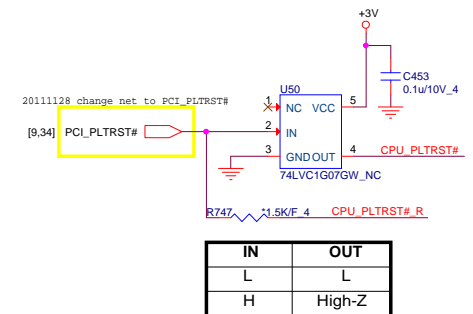
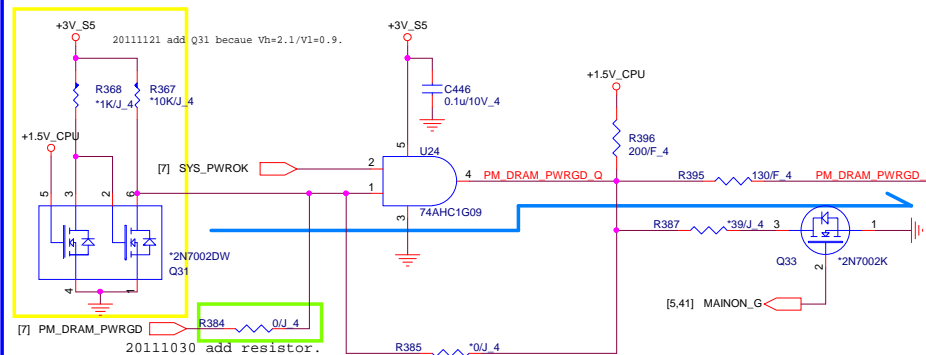
XDP_TMS_VT R739 51/J_4
XDP_TDI_VT R755 51/J_4
XDP_PREQ# R738 *51/J_4

XDP_TCLK_VT R746 51/J_4
XDP_TRST# R744 51/J_4
When MP, JTAG PU/PD resistor can be removed? (Yes Intel, TDI, TDO, TMS, TRST#, TCK, PREQ#, PRDY#)

Thermal Trip (CPU)

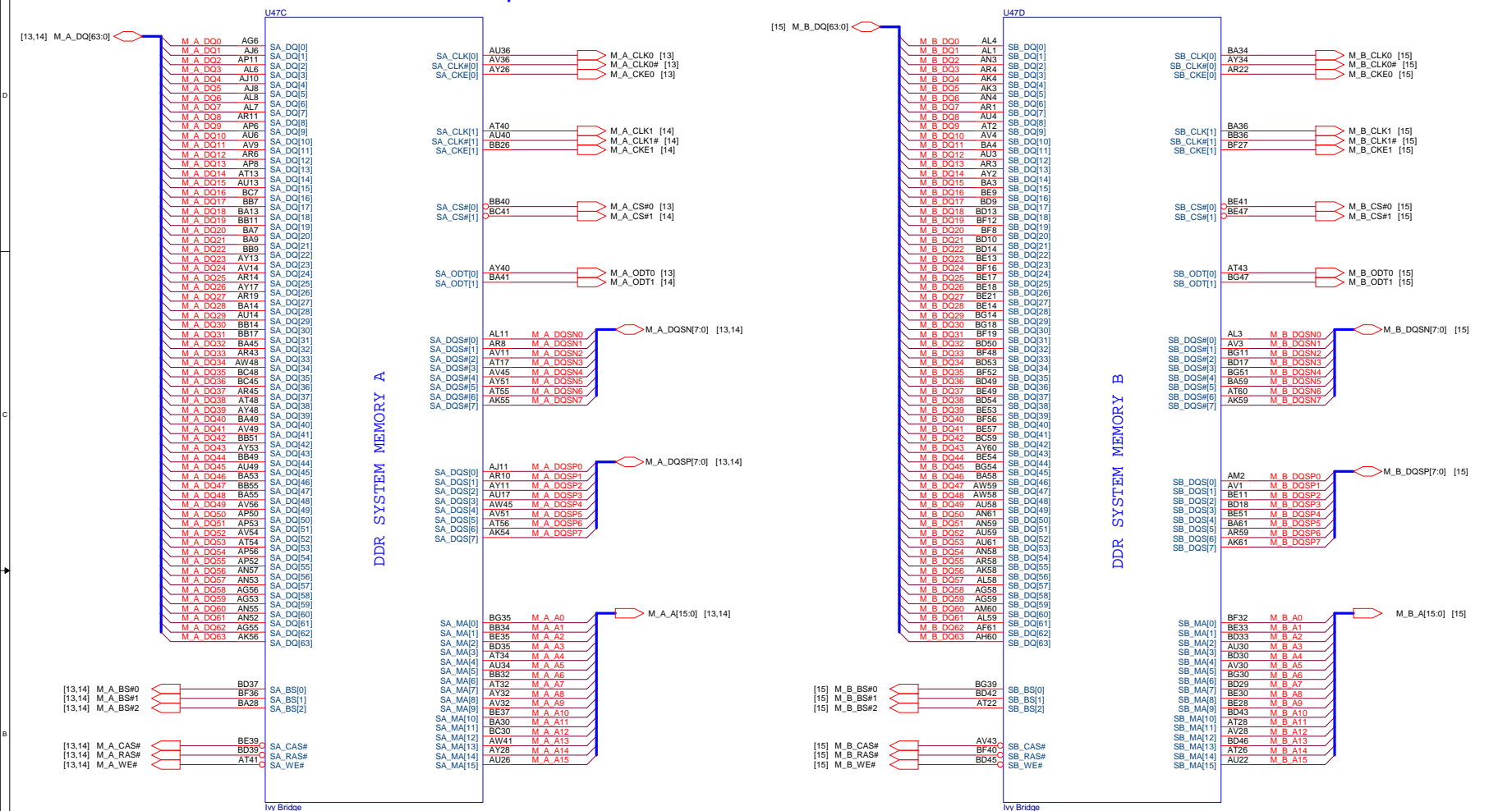


S3 leakage circuit (CPU)



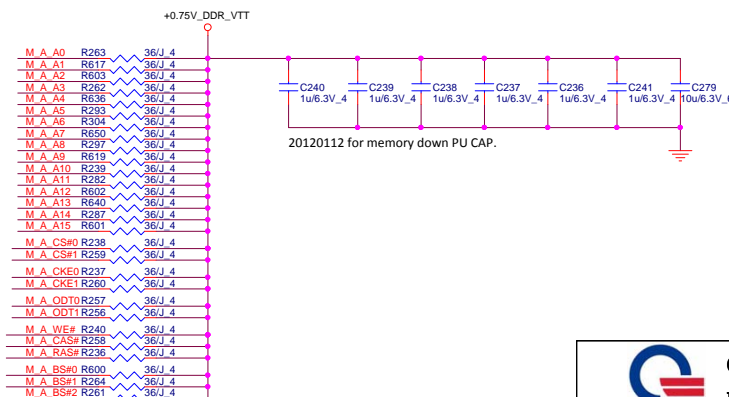
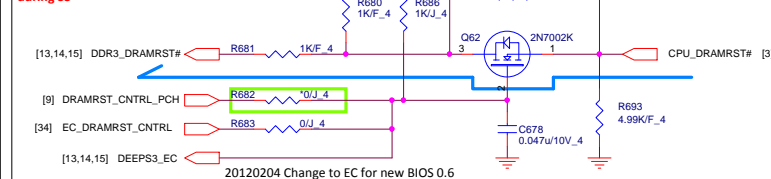
Channel A: On board RAM 2Rx16 8pcs

Channel B: SO-DIMM



S3 leakage circuit (CPU)

S3 circuit: DRAM_RST# to memory should be high during S3



IVY Bridge Processor (POWER) (CPU)

CPU VCCIO
IVY 17W:8.5A
Cose down
330uF/6mohm x 2 330uF/6mohm x 1
10uF x 10 10uF x 10
1uF x 26 1uF x 26

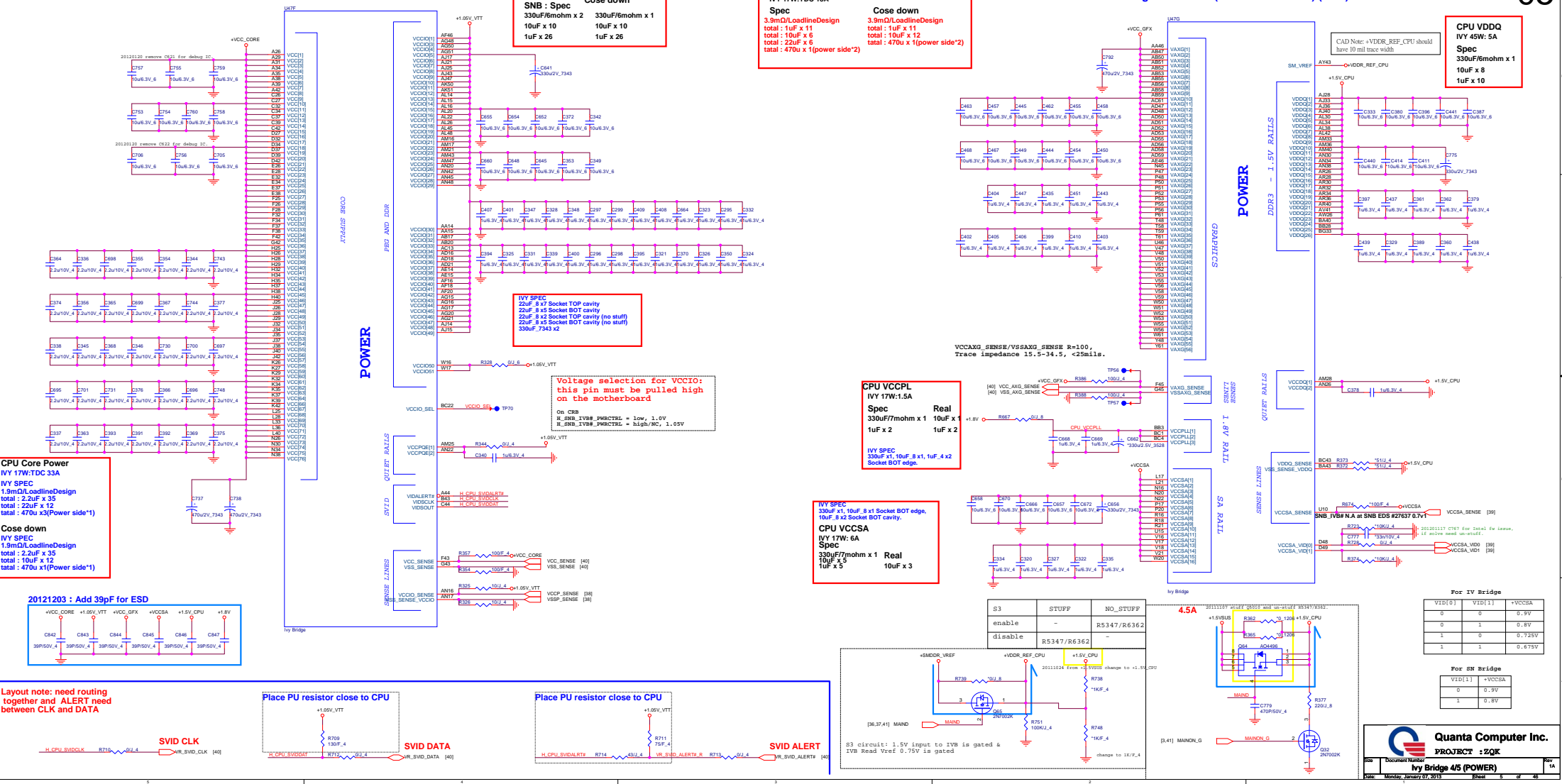
CPU VCCAXG
IVY 17W:TDC 18A
Spec
3.9mD/LoadlineDesign
total : 1uF x 11
total : 10uF x 12
total : 22uF x 6
total : 470u x 1 (power side*2)

Cose down
3.9mD/LoadlineDesign
total : 1uF x 11
total : 10uF x 12
total : 470u x 1 (power side*2)

IVY Bridge Processor (GRAPHIC POWER) (GPU)

CPU VDDQ
IVY 45W: 5A
Spec
330uF/6mohm x 1
10uF x 8
1uF x 10

CAD Note: +VDDR_REF_CPU should have 10 mil trace width



CPU Core Power
IVY 17W:TDC 33A
IVY SPEC
1.9mD/LoadlineDesign
total : 2.2uF x 35
total : 22uF x 12
total : 470u x 3 (Power side*)

Cose down
IVY SPEC
1.9mD/LoadlineDesign
total : 2.2uF x 35
total : 10uF x 12
total : 470u x 1 (Power side*)

IVY SPEC
22uF 8 x5 Socket TOP cavity
22uF 8 x5 Socket BOT cavity (no stuff)
22uF 8 x5 Socket TOP cavity (no stuff)
330uF_7343 x2

Voltage selection for VCCIO:
this pin must be pulled high on the motherboard

On CB8
H_SNS_VB8_FMRCTEL = low, 1.0V
H_SNS_VB8_FMRCTEL = high/MC, 1.05V

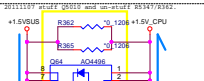
CPU VCCPL
IVY 17W:1.5A
Spec
330uF/7mohm x 1 10uF x 1
1uF x 2 1uF x 2

IVY SPEC
330uF x1, 10uF 8 x1, 1uF 4 x2
Socket BOT edge.

IVY SPEC
330uF x1, 10uF 8 x1 Socket BOT edge,
10uF 1 x2 Socket BOT cavity.

CPU VCCSA
IVY 17W: 6A
Spec
330uF/7mohm x 1 Real
10uF x 5 10uF x 3

| S3 | STUFF | NO_STUFF |
|---------|-------------|-------------|
| enable | - | R5347/R6362 |
| disable | R5347/R6362 | - |



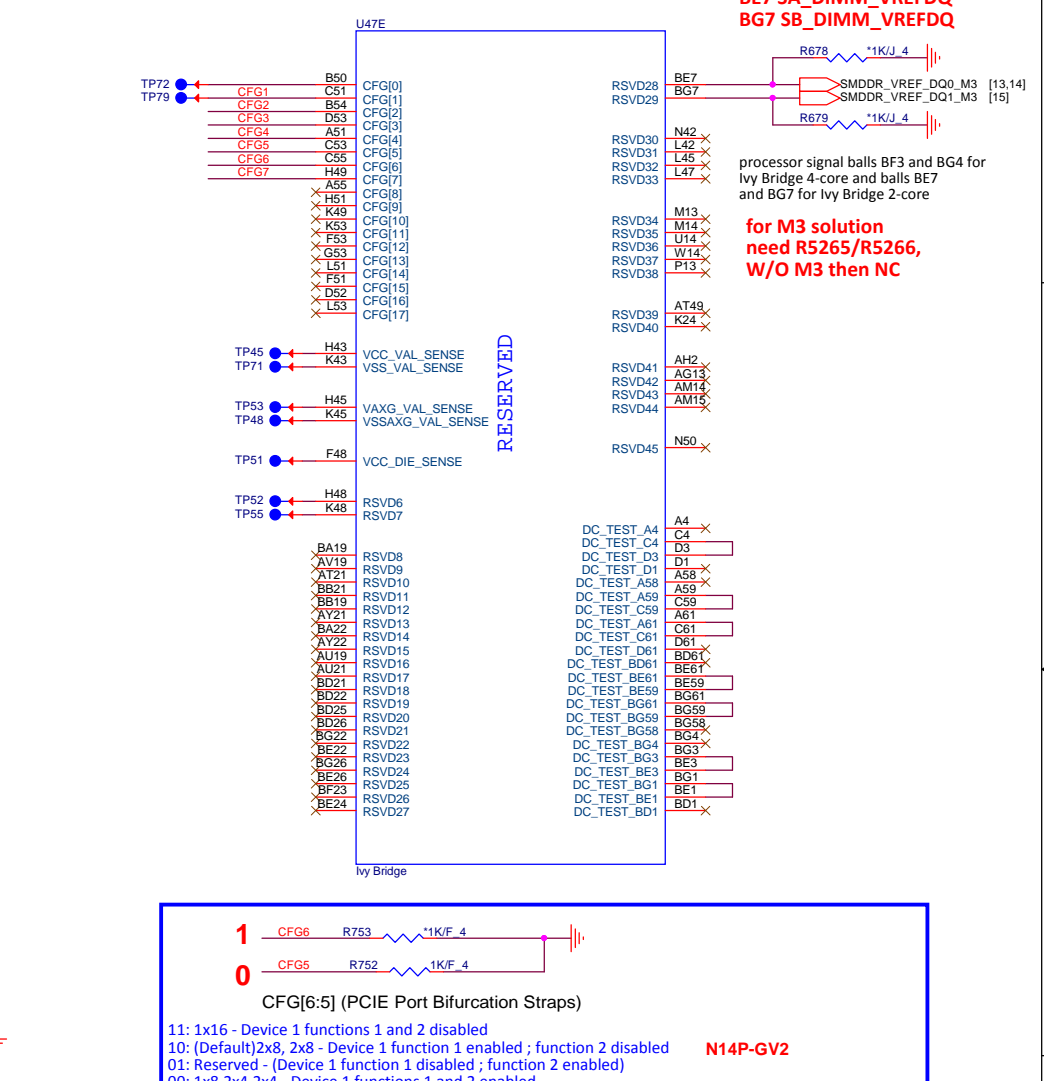
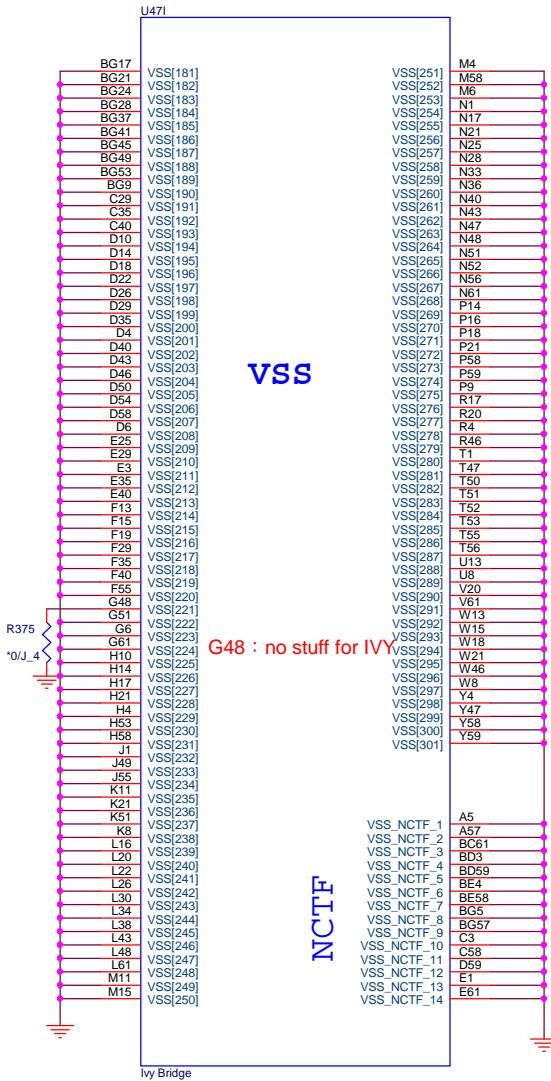
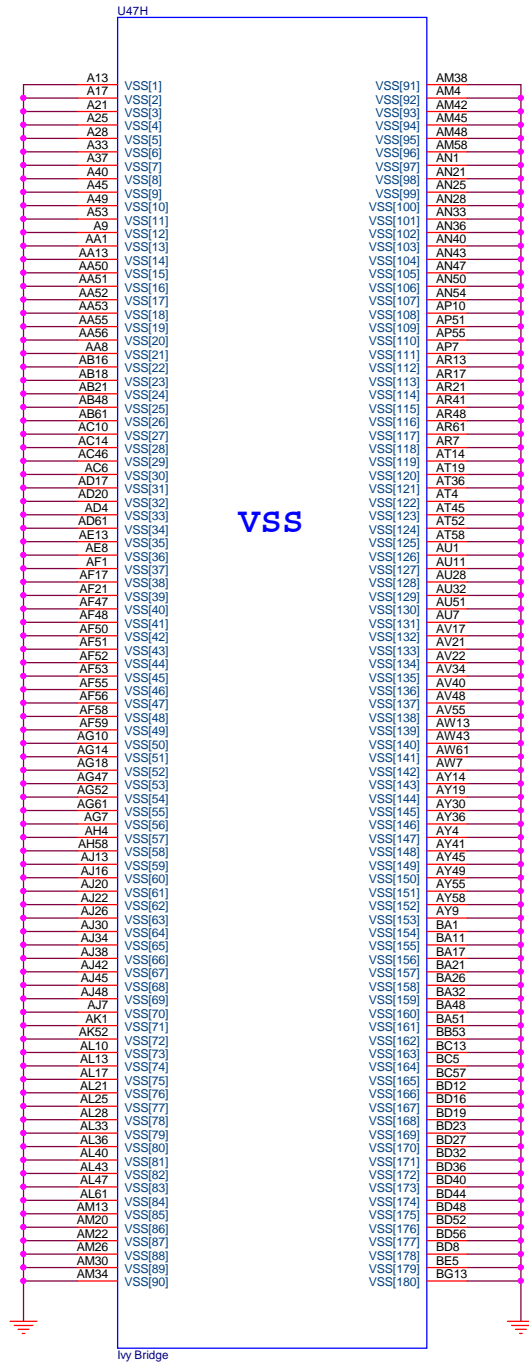
| For IV Bridge | | |
|---------------|--------|--------|
| VID[0] | VID[1] | +VCCSA |
| 0 | 0 | 0.9V |
| 0 | 1 | 0.8V |
| 1 | 0 | 0.725V |
| 1 | 1 | 0.675V |

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IVY Bridge Processor (GND) (CPU)

IVY Bridge Processor (RESERVED, CFG) (CPU)

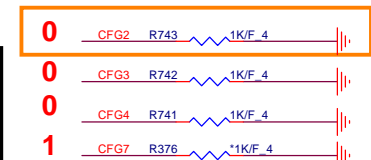
BE7 SA_DIMM_VREFDQ
BG7 SB_DIMM_VREFDQ



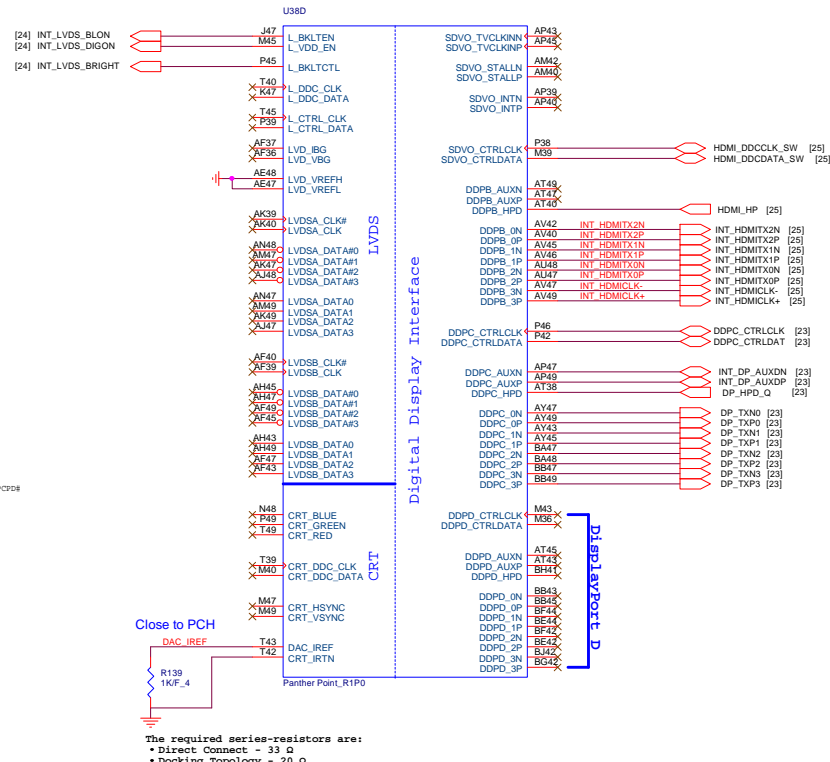
Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

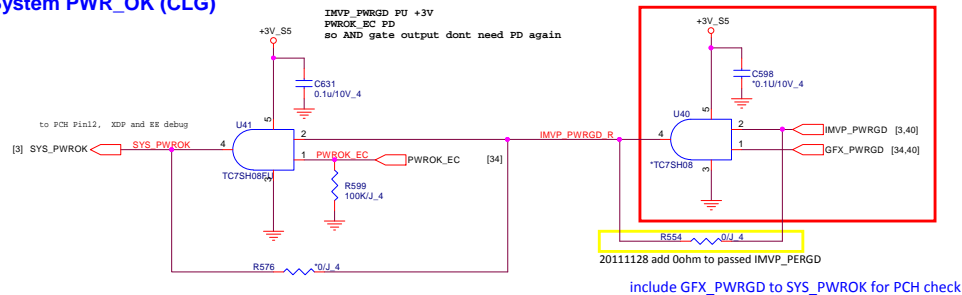
| | 1 | 0 |
|--|--|--|
| CFG2 (PCI-E Static x16 Lane Reversal) | Normal Operation | Lane Reversed |
| CFG3 (PCI-E Static x4 Lane Reversal) | Normal Operation | Lane Reversed |
| CFG4 (DP Presence Strap) | Disable; No physical DP attached to eDP | Enable; An ext DP device is connected to eDP |
| CFG7 (PEG Defer Training) | PEG train immediately following xxRESETB de assertion | PEG wait for BIOS training |



CPT/PPT (LVDS,DDI)



System PWR_OK (CLG)



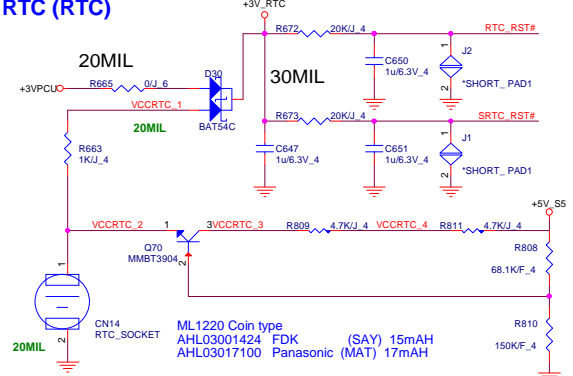
[34] APWROK

R607 0Ω/J_4

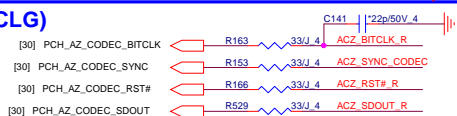
APWROK_R

R608 100K/J_4

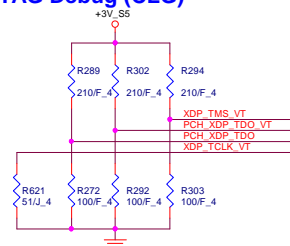
RTC (RTC)



HDA Bus (CLG)

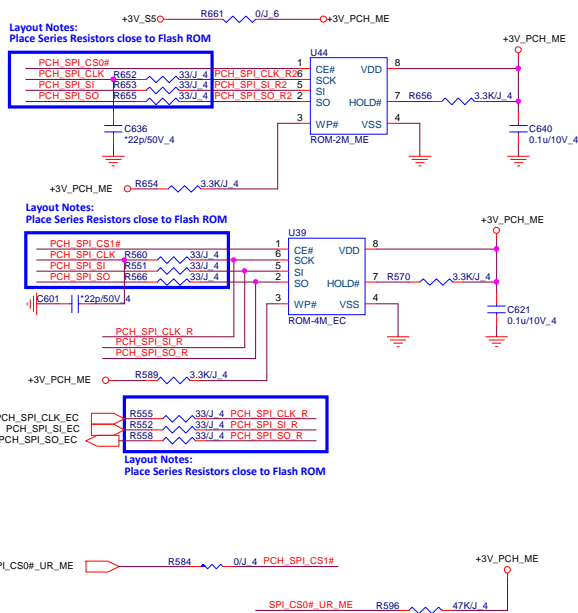


PCH JTAG Debug (CLG)

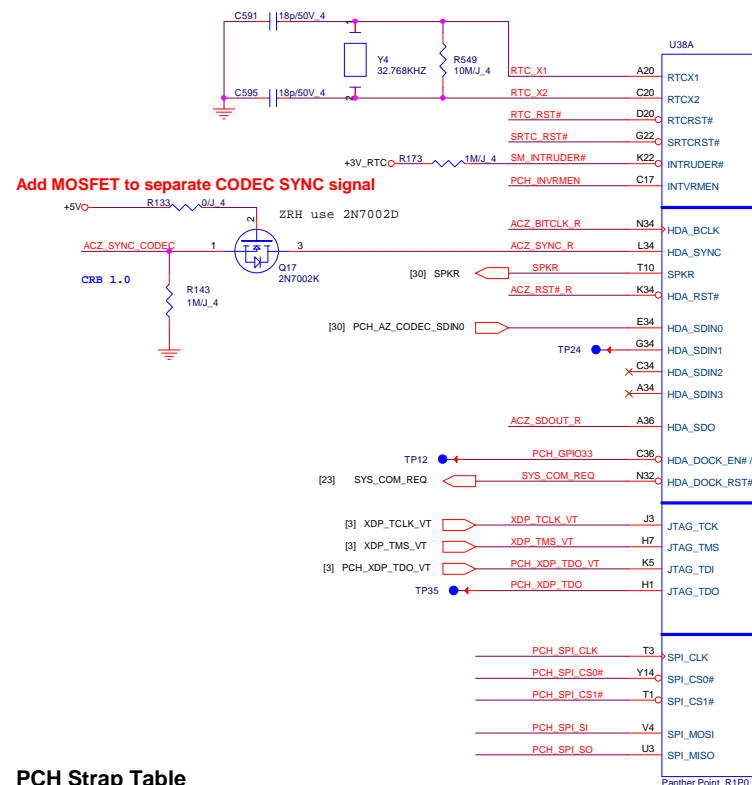


PCH Dual SPI (CLG) (Default for WIN8)

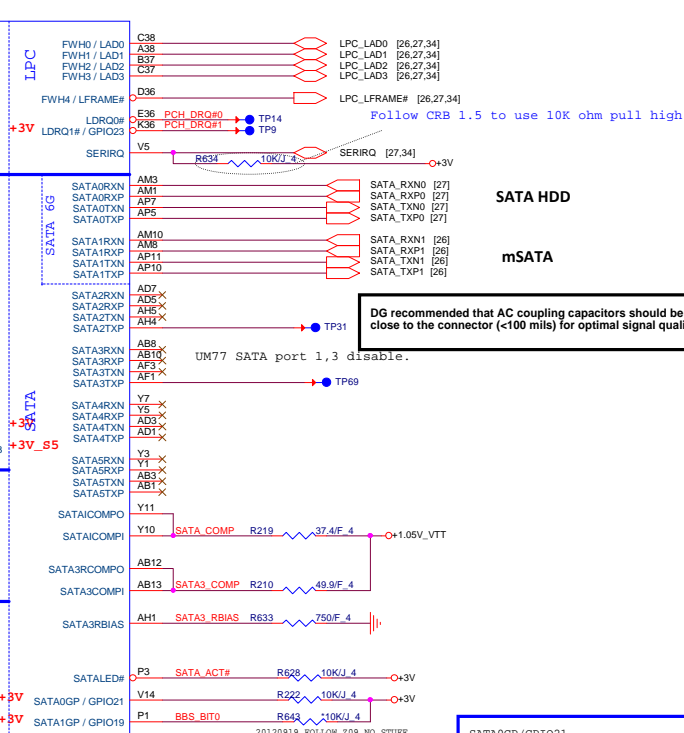
```
W25Q32BVSSIG / AKE391P0N00----->4MB
W25Q16BVSSIG / AKE38FP0N01----->2MB
```



PCH2 (CLG)



CPT/PPT (HDA,JTAG,SATA) (CLG)



DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

SATA HDD

mSATA

PCH Strap Table

| Pin Name | Strap description | Sampled | Configuration | | | | | | | | | | |
|----------------|---|---------------|--|-------|--------|---------------|---|---|-------|---|---|-----|--|
| SPKR | No reboot mode setting | PWROK | 0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode | | | | | | | | | | |
| GNT3# / GPIO55 | Top-Block Swap Override | PWROK | 0 = "top-block swap" mode 1 = Default (weak pull-up 20K) | | | | | | | | | | |
| INTVRMEN | Integrated 1.05V VRM enable | ALWAYS | Should be always pull-up | | | | | | | | | | |
| GNT1# / GPIO51 | Boot BIOS Selection 1 [bit-1] | PWROK | <table border="1"><thead><tr><th>GNT1#</th><th>GPIO19</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></tbody></table> | GNT1# | GPIO19 | Boot Location | 1 | 1 | SPI * | 0 | 0 | LPC | |
| GNT1# | GPIO19 | Boot Location | | | | | | | | | | | |
| 1 | 1 | SPI * | | | | | | | | | | | |
| 0 | 0 | LPC | | | | | | | | | | | |
| GPIO19 | Boot BIOS Selection 0 [bit-0] | PWROK | | | | | | | | | | | |
| HDA_SDO | Flash Descriptor Security | RSMRST | 0 = effect (default)(weak pull-down 20K) 1 = overridden | | | | | | | | | | |
| DF_TVS | DMV/FDI Termination voltage | PWROK | 0 = Set to Vss (weak pull-down 20K) 1 = Set to Vcc | | | | | | | | | | |
| GPIO28 | On-die PLL Voltage Regulator | RSMRST# | 0 = Disable 1 = Enable (weak pull-up 10K) | | | | | | | | | | |
| HDA_SYNC | On-Die PLL VR Voltage Select | RSMRST | 0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V | | | | | | | | | | |
| GPIO15 | Intel ME Crypto Transport Layer Security (TLS) cipher suite internal PD | RSMRST | 0 = Disable (Default) 1 = Enable | | | | | | | | | | |
| DSWVREN | DEEP S4/S5 well On Die DSW VR Enable | DSW | High = Enable (Default) Low = Disable | | | | | | | | | | |
| NV_ALE | Intel Anti-Theft HDD protection Only for Interposer | PWROK | 0 = Disable (Internal pull-down 20kohm) | | | | | | | | | | |

Used as GPIO only. at chklist 1.2

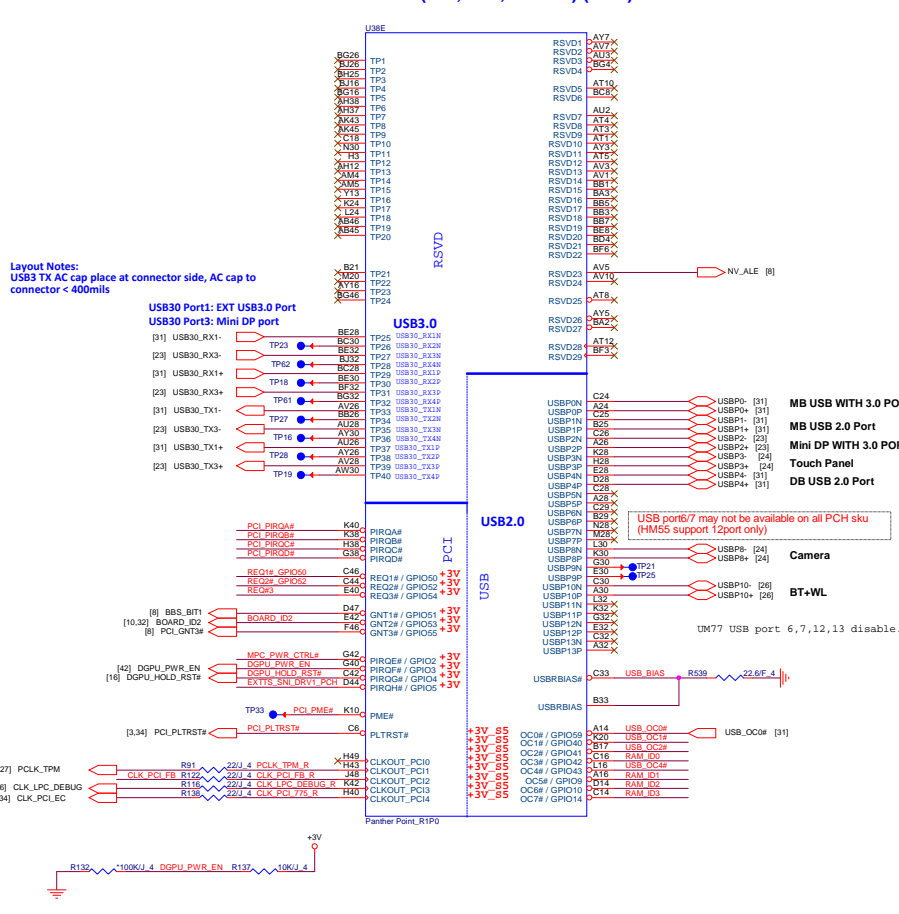
Default weak pull-up on GNT0/1#
[Need external pull-down for LPC BIOS]

ME WR default EC setting folating

for future CPU, Sandy Bridge NC
DF_TVS needs to be pulled up to VccDFTERM power rail
through 2.2 kOhm $\pm 5\%$ - R8361 change to 0 or not??

Needs to be pulled High for Chief River platform
chklist 2.0

CPT/PPT (PCI,USB,NVRAM) (CLG)



PCIE port 1 for commercial model S3 can't weak up.

Wireless

[26] PCIE_RX8+
[26] PCIE_RX8-
[26] PCIE_TX8+
[26] PCIE_TX8-

LAN

[28] PCIE_RXN3_LAN
[28] PCIE_RXP3_LAN
[28] PCIE_TXN3_LAN
[28] PCIE_TXP3_LAN

UM77/BM70 will disable 5-8 PCIE ports

RT

RT

EHC11

USB Port1 can be used on debug mode
XHCI for USBP0-3

EHC12

USB Port9 can be used on debug mode
1001 : (BIOS) Use port1 is enough

20110908 WLAN support S3 wake up function.

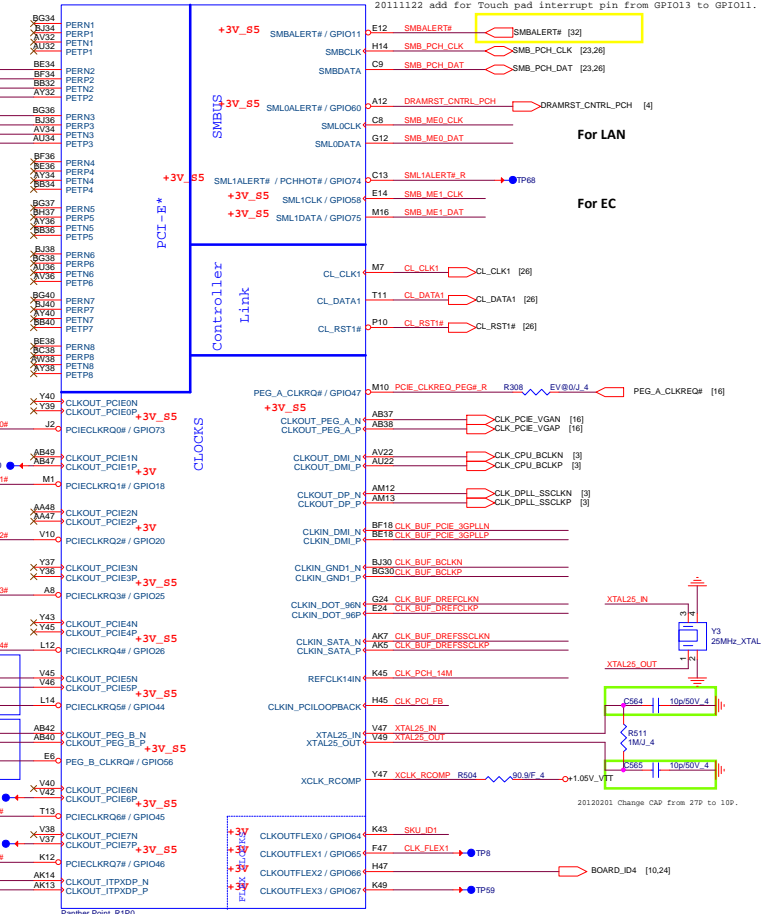
Wireless

[26] CLK_PCIE_WLAN#
[26] CLK_PCIE_WLAN
[28] CLK_PCIE_WLAN_REQ#

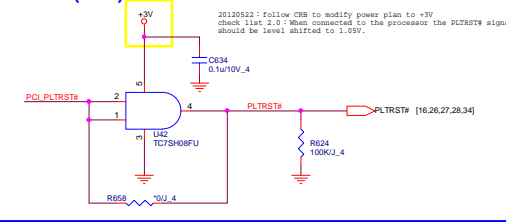
LAN

[28] CLK_PCIE_LANN
[28] CLK_PCIE_LANP
[28] CLK_PCIE_LAN_REQ#

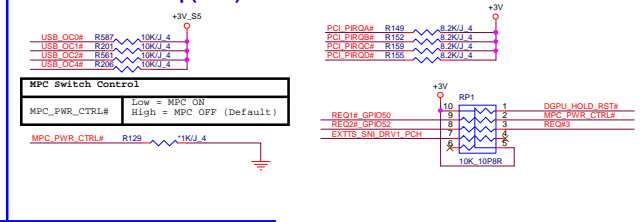
TP10
TP17



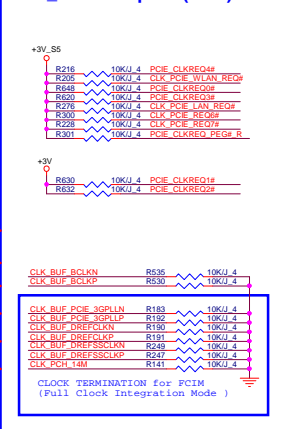
PLTRST#(CLG)



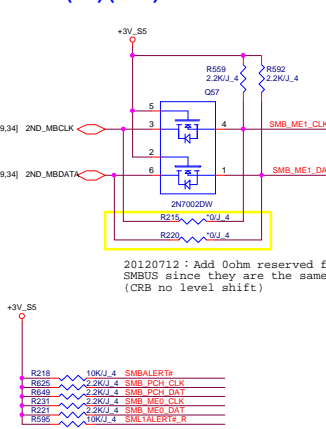
PCI/USBOC# Pull-up(CLG



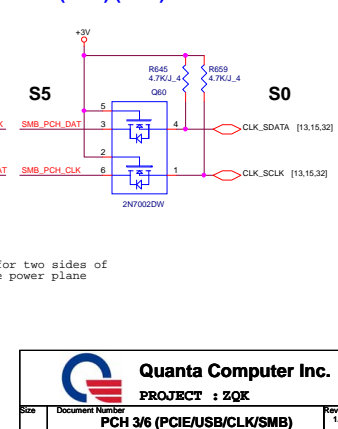
| | |
|------------------------|-----------------|
| CLK_REQ/Strap Pin(CLG) | SMBus(EC) (CLG) |
|------------------------|-----------------|



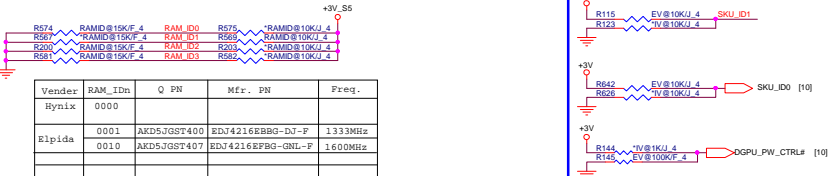
SMBus(EC) (CLG)



SMBus(PCH) (CLG)



DDRIII Memory down strap (CLG)



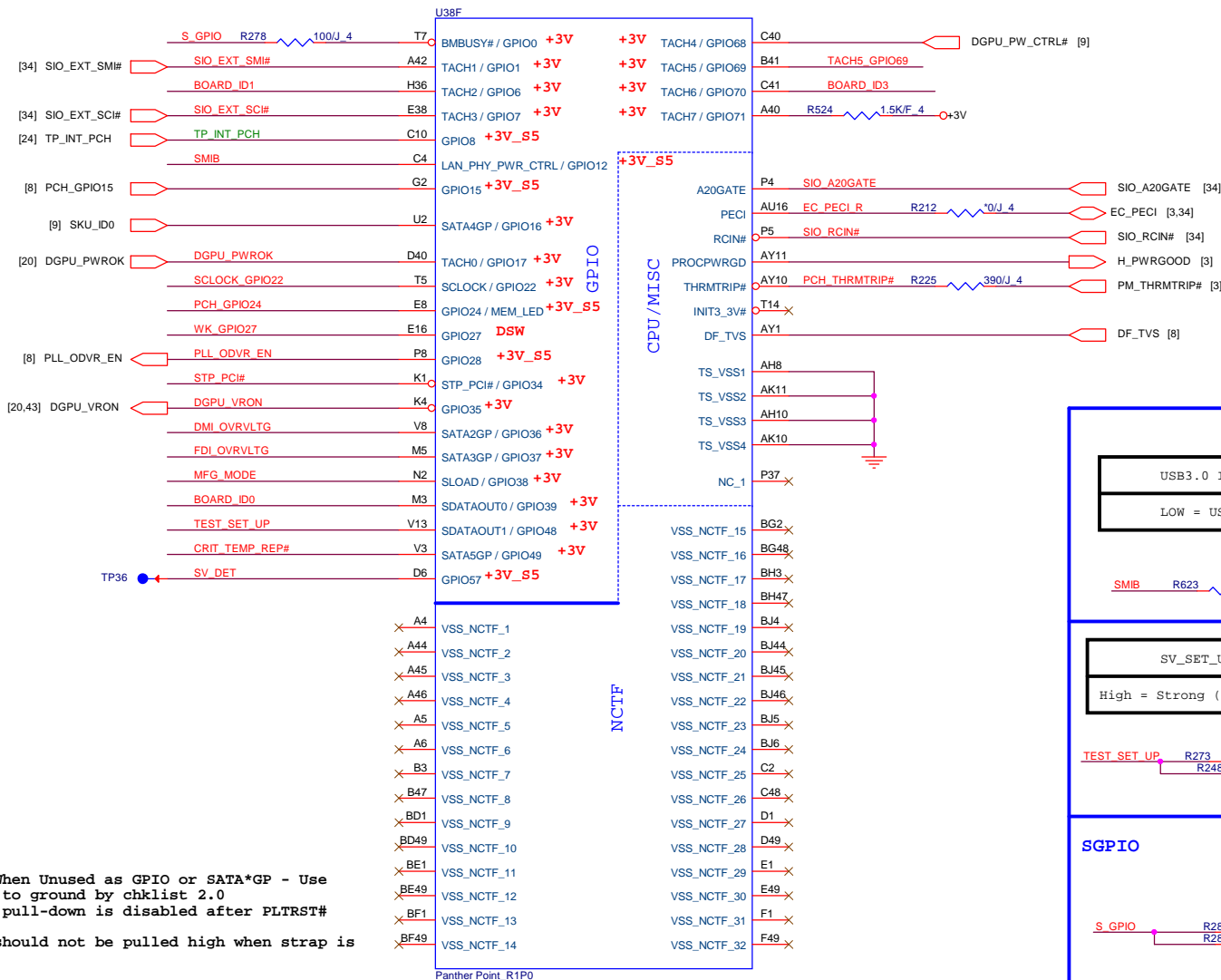
| | GPU_PW_CTRL# (CPU#0) | GPU_101 (CPU#0) | GPU_102 (CPU#0) | V/A HW Signal | Setup Menu |
|-----------------------|-------------------------|--------------------|--------------------|------------------|---------------|
| UMA Only | 1 | 0 | 0 | UMA | Hidden |
| dGPU Only | 0 or 1 | 0 | 1 | GPU | Hidden |
| Switchable (Huc) | 0 | 1 | 0 | UMA+dGPU | dGPU/SG |
| Optimize (Hucless) | 0 | 1 | 1 | UMA/SG | UMA |

dGPU_PW_CTRL#
 1 = GPU power is control by H/W (Pure Discrete SKU)
 0 = GPU power is control by PCH GPIO (Discrete, SG or Optimize)

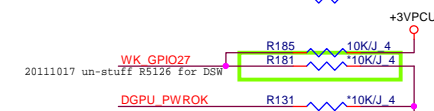
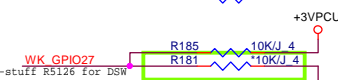
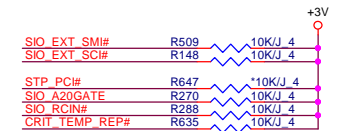
CPT/PPT (GPIO,VSS_NCTF,RSVD) (CLG)

10

GPIO Pull-up/Pull-down (CLG)



20120625 : <PCH_GPIO24>Follow CRB to pull up 10K ohm



GPIO27 : If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

USB3.0 IC CTL

LOW = USB3.0 IC

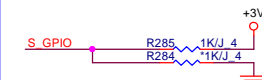


SV_SET_UP

High = Strong (Default)



SGPIO

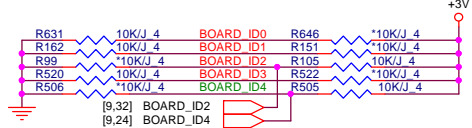
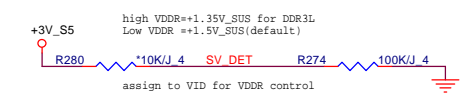
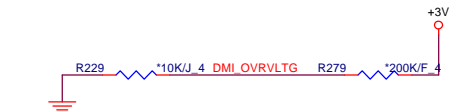


MFG-TEST



DMI TERMINATION VOLTAGE OVERRIDE

Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)



| High | Low |
|-----------|---------------------------------------|
| BOARD_ID0 | GDDR5 |
| BOARD_ID1 | Disable on board memory |
| BOARD_ID2 | Pin8 of SYNAPTICS and ELAN are NC pin |
| BOARD_ID3 | Default is pull high |
| BOARD_ID4 | BIOS maybe will use EEPROM detection |
| | No touch panel |
| | Touch panel |

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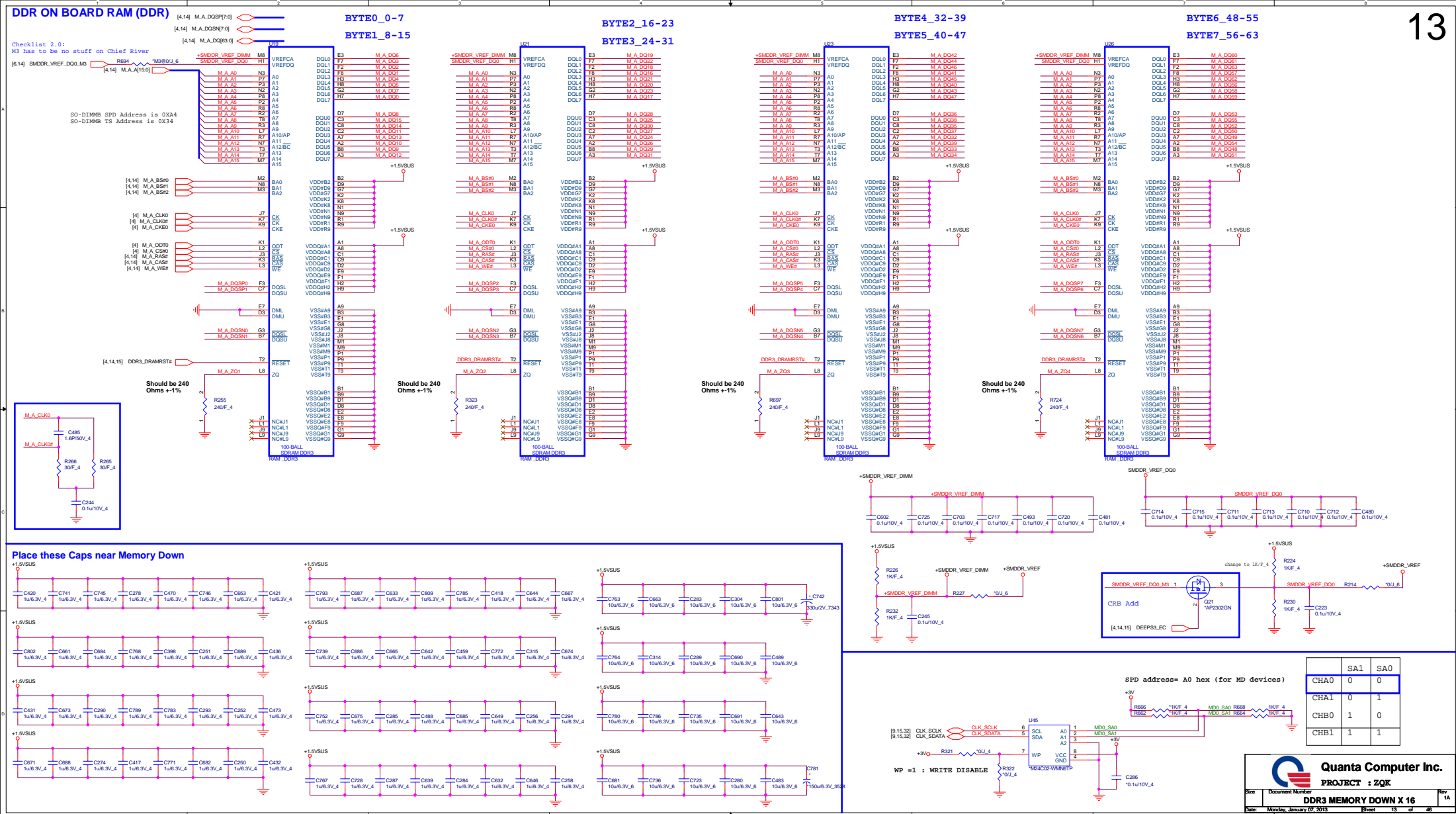
PROJECT : ZQK

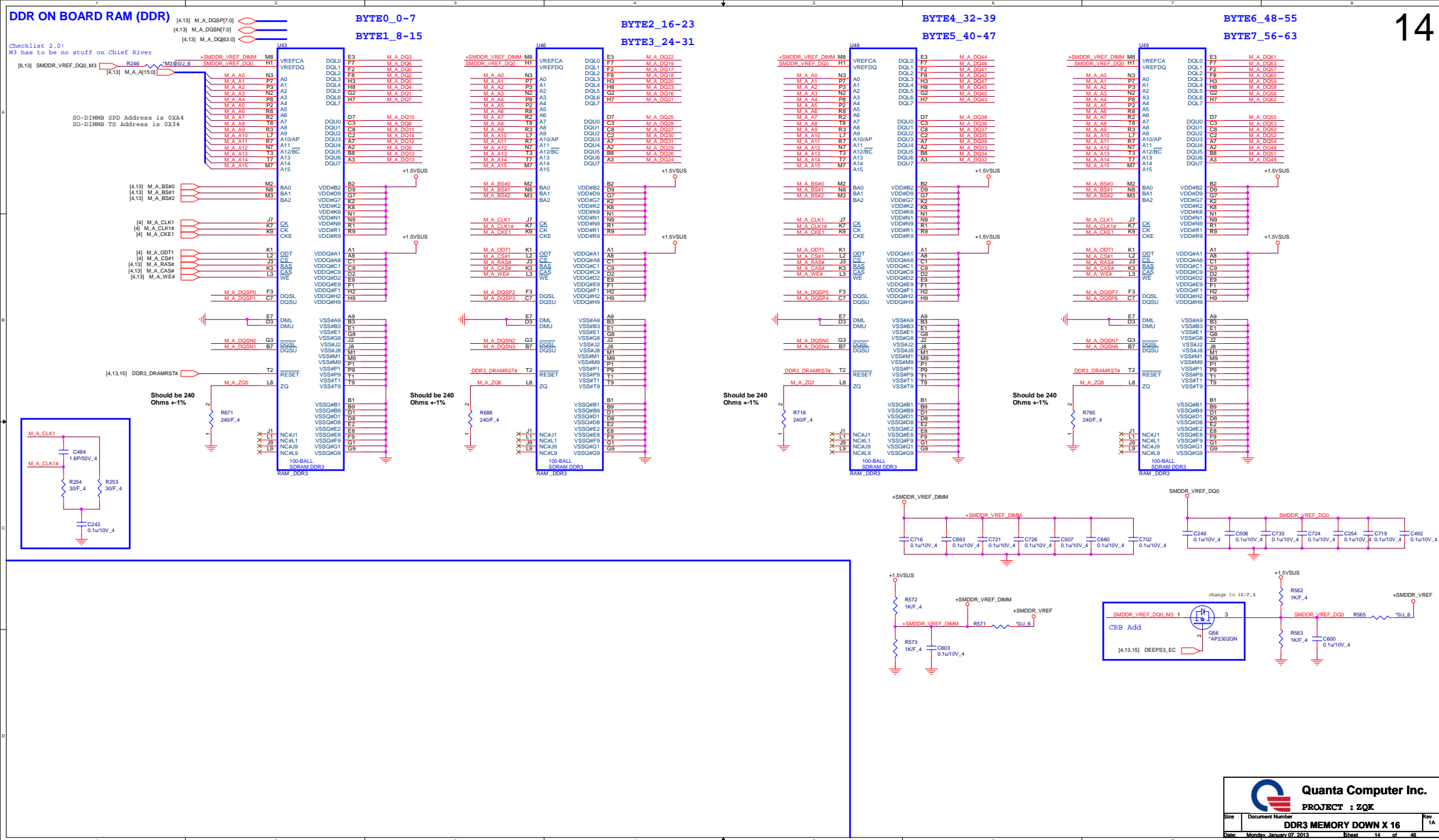
PCH 4/6 (GPIO/MISC)

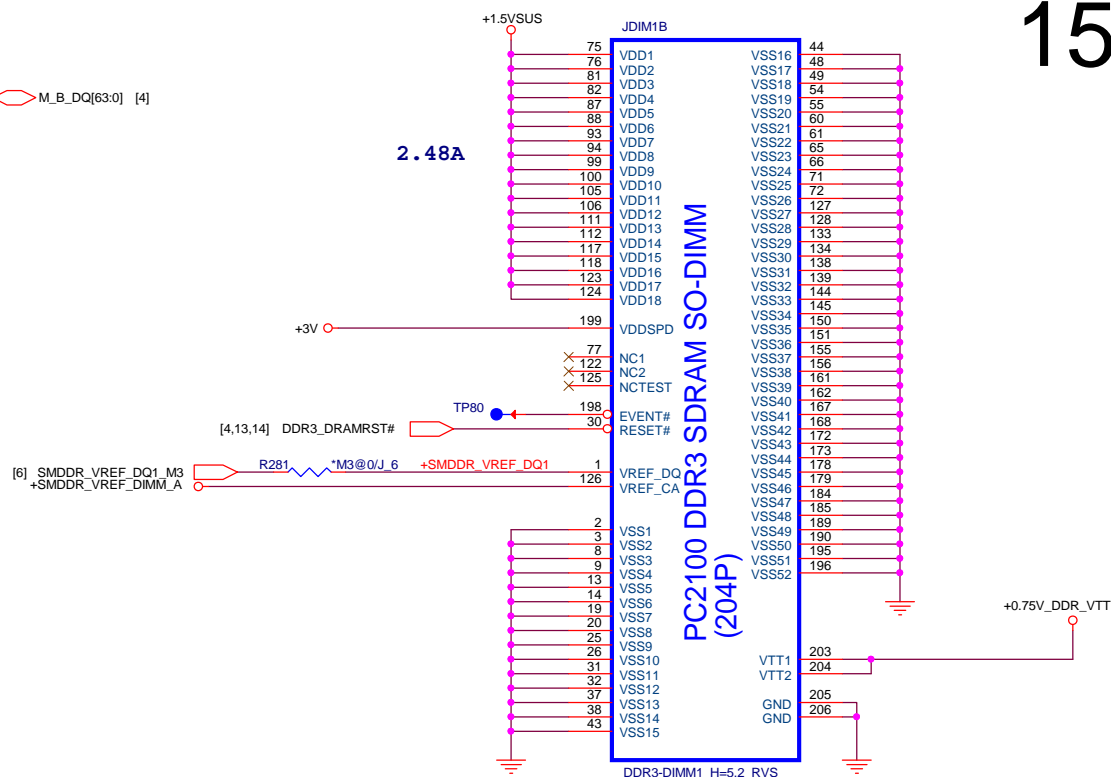
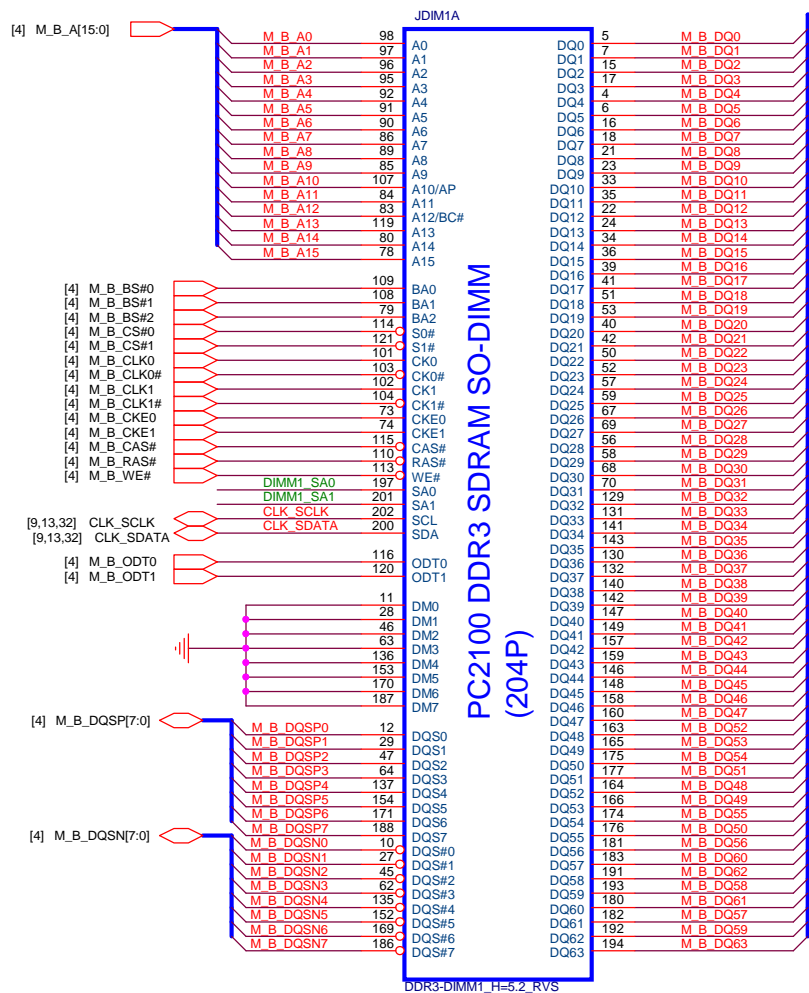
Size Document Number Rev 1A

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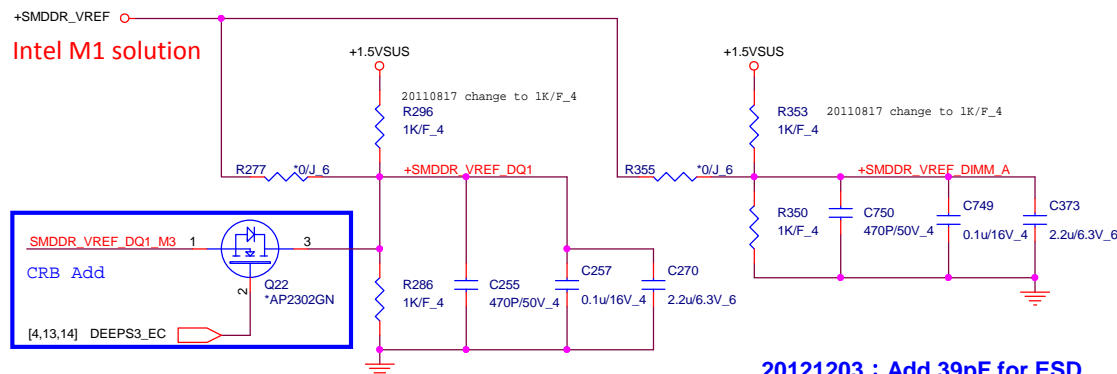




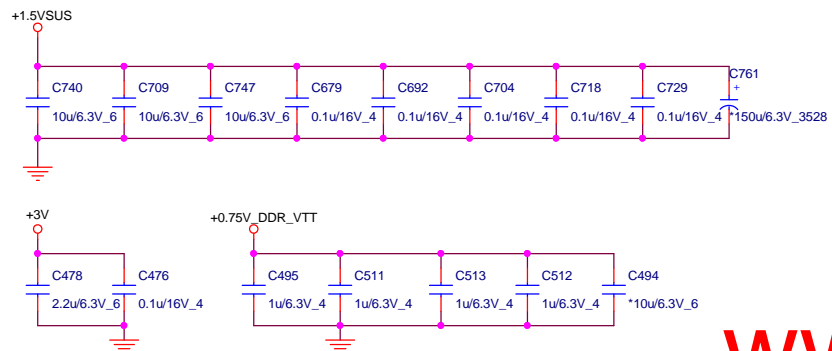




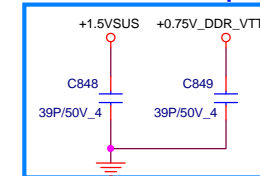
Intel M1 solution



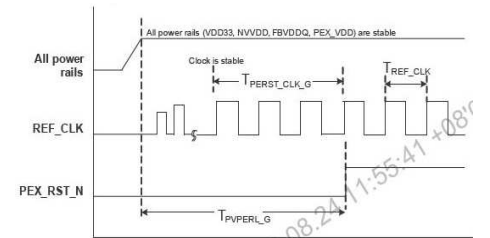
Place these Caps near SO_DIMM-A



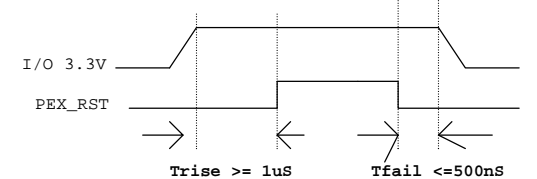
20121203 : Add 39pF for ESD

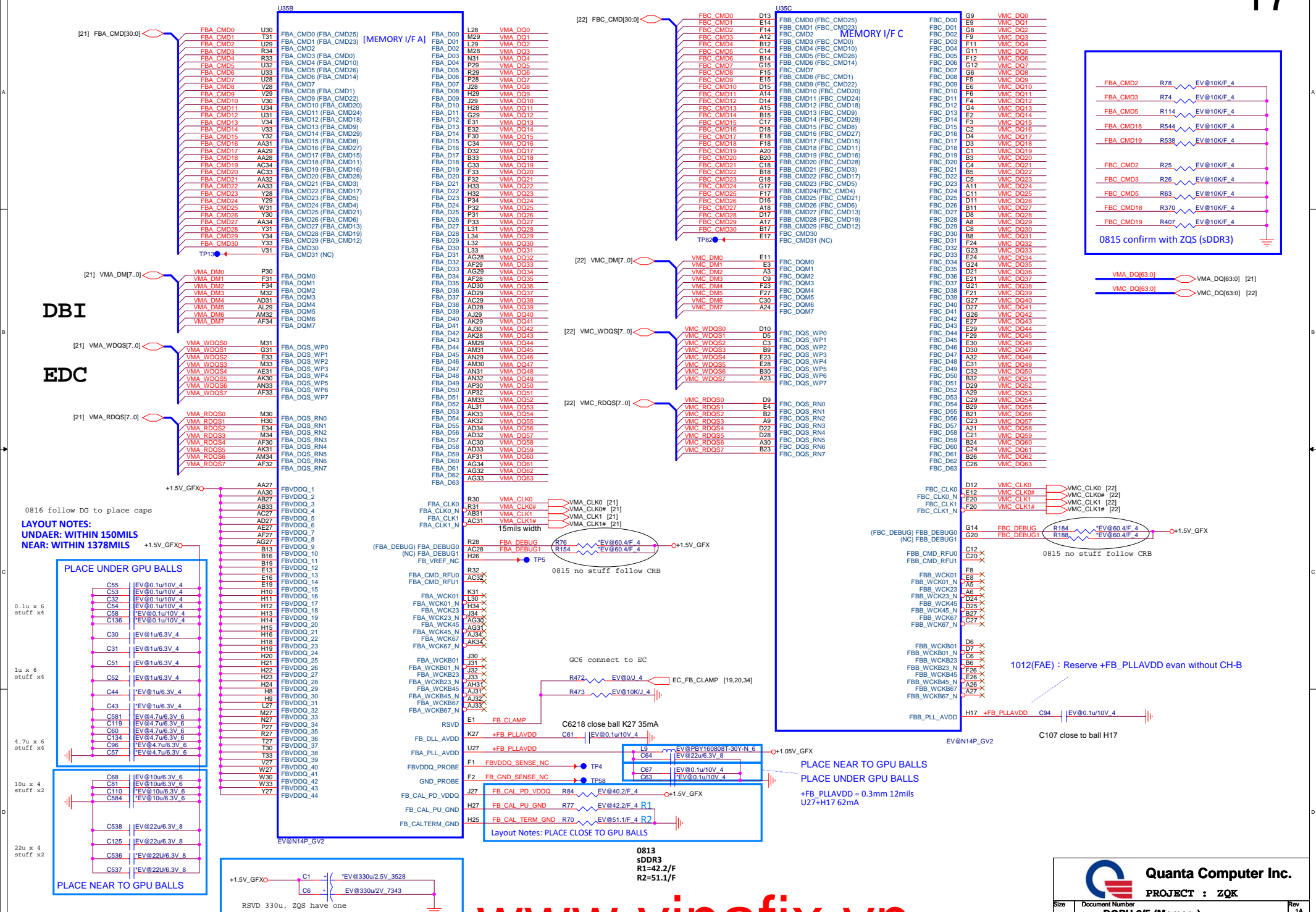


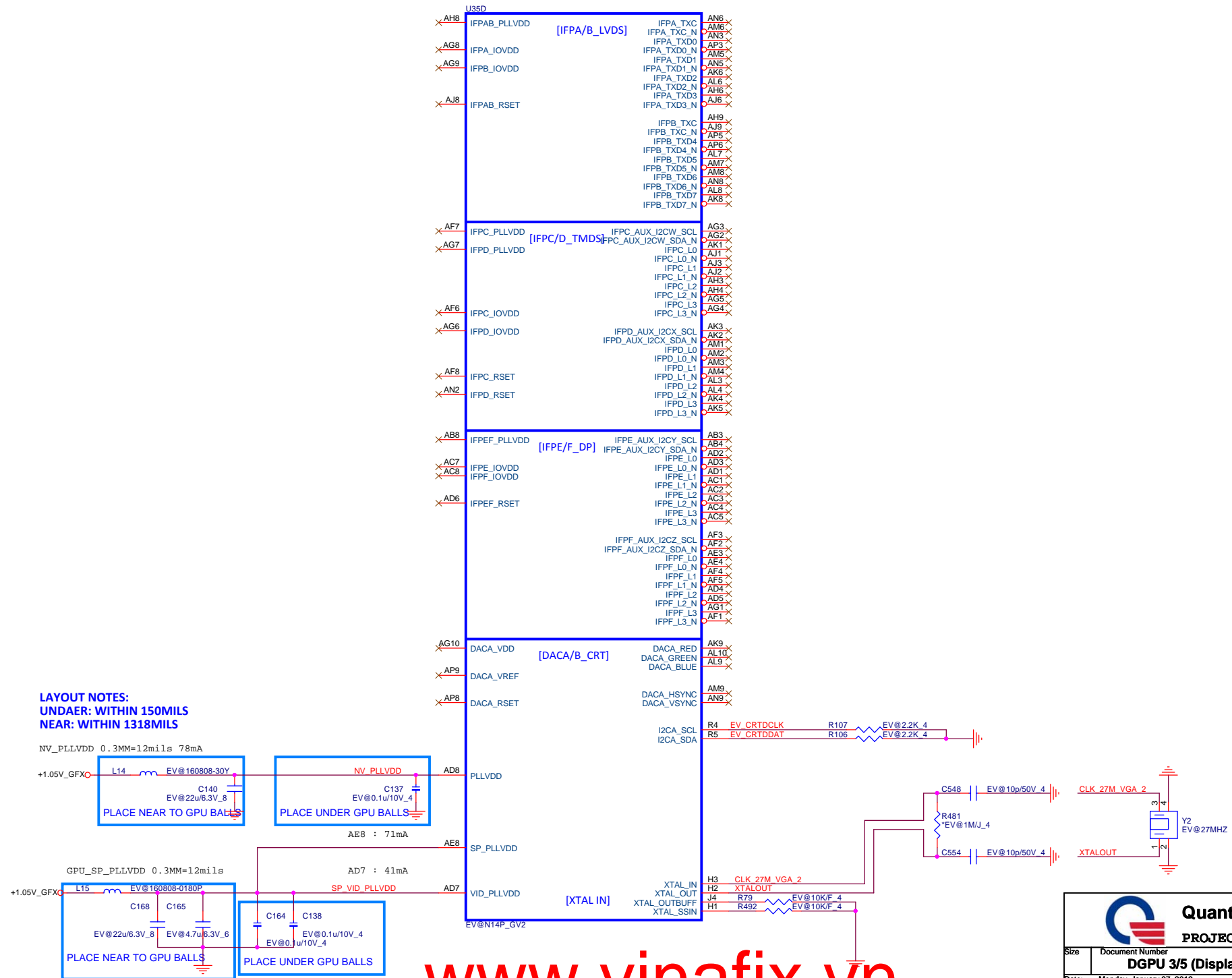
| | SA1 | SA0 |
|------|-----|-----|
| CHA0 | 0 | 0 |
| CHA1 | 0 | 1 |
| CHB0 | 1 | 0 |
| CHB1 | 1 | 1 |



| Constraint Parameter | Requirement | Notes |
|----------------------|--|-------|
| T_FVTERL_G | $T_{FVTERL_G} \geq 1\mu s$ | |
| T_FERST_CLK_G | $T_{FERST_CLK_G} \geq 1T_{REF_CLK}$ | |







Logical Strap Bit Mapping

| | PU-VDD | PD |
|-------|--------|------|
| 4.99K | 1000 | 0000 |
| 10K | 1001 | 0001 |
| 15K | 1010 | 0010 |
| 20K | 1011 | 0011 |
| 24.9K | 1100 | 0100 |
| 30.1K | 1101 | 0101 |
| 34.8K | 1110 | 0110 |
| 45.3K | 1111 | 0111 |

Logical Strapping Bit3

| Logical Strapping Bit3 | Logical Strapping Bit2 | Logical Strapping Bit1 | Logical Strapping Bit0 |
|------------------------|------------------------|------------------------|------------------------|
| ROM_SO | FB_1 | FB_0 | SMB_ALT_ADDR |
| ROM_SCLK | PCI_DEVID[4] | SUB_VENDOR | PCI_DEVID[5] |
| ROM_S1 | RAMCFG[3] | RAMCFG[2] | RAMCFG[1] |
| STRAP0 | USER[3] | USER[2] | USER[1] |
| STRAP1 | 3GIO_PADCFG[3] | 3GIO_PADCFG[2] | 3GIO_PADCFG[1] |
| STRAP2 | PCI_DEVID[3] | PCI_DEVID[2] | PCI_DEVID[1] |
| STRAP3 | SOR3_EXPOSED | SOR2_EXPOSED | SOR0_EXPOSED |
| STRAP4 | RESERVED | PCI_SPEED_CHANGE_GEN3 | PCI_MAX_SPEED |

STRAP3

| | |
|---------------|------------|
| Optimus | → 4.99K PD |
| Discrete only | → 15K PD |

Table 123 Binary Strap Mode Mapping

| Strap Pin Name | Strap Mapping | Resistance | Polarity |
|----------------|----------------|------------|--|
| ROM_SCLK | SMB_ALT_ADDR | 10k Ω | Pull down to GND |
| ROM_S1 | SUB_VENDOR | 10k Ω | Pull up to 3V3 if VBIOS ROM exists Pull down to GND if no VBIOS ROM |
| ROM_SO | VGA_DEVICE | 10k Ω | Pull down to GND (no display) |
| STRAP0 | RAM_CFG[0] | 10k Ω | See Note below |
| STRAP1 | RAM_CFG[1] | 10k Ω | See Note below |
| STRAP2 | RAM_CFG[2] | 10k Ω | See Note below |
| STRAP3 | RAM_CFG[3] | 10k Ω | See Note below |
| STRAP4 | PCIE_MAX_SPEED | 10k Ω | Pull down to GND |

N14M-GE device ID is 0x1140
N14M-GE is use binary strap setting

A.ROM_S1 - 10k pull down
B.ROM_SO - 10k pull down
F.STRAP 3 - 10k pull down

Micron: MT41K256M16HA-107G:E (QPN = AKD5PGSTL05)
strap = 0xD = (0x1101)
STRAP 3&2&0 = 10K Pull high
STRAP 1 = 10K Pull down

A.ROM_S1 - Memory strap

B.ROM_SO - 5K pull high

D.STRAP 0 - 45K pull high

E.STRAP 1 - GV2 - 45K pull down

F.STRAP 3 - 5K pull down

C2.For N14P-GV2+SDR3 sku

N14P-GV2 OS device ID=0x1292 'This is QS device ID

1.ROM_SCLK = 5K pull high

2.STRAP2 = 15K pull down

3.STRAP4 = 45K pull down For N14P-GV2 QS

N14P-GT device ID=0x0FE4

1.ROM_SCLK = 15K pull down

2.STRAP2 = 25K pull down

5.STRAP4 = 45K pull down

Table 3. N14M-GS/LP and N14P-GV2 DDR3 Recommended Memories 128Mx16 Configuration

| Configuration | Vendor | Strap | FBVDD/ FBVDDQ | Manufacturer Part Number | Max Speed CK (MHz) | Memory Date Code Minimum | Status |
|---------------|---------|-------|------------------|-----------------------------|-----------------------------|--------------------------------|-------------------------|
| 128Mx16 DDR3 | Samsung | 0x7 | 1.5 V/ 1.5 V | K4V2G1646E-BC11 | 1000 | 1204 | Production Candidate |
| | | | 1.5 V/ 1.5 V | MT41J128M16JT-107G-E | 1000 | 1150 | Production Candidate |
| | Hynix | 0x5 | 1.5 V/ 1.5 V | MT41J128M16JT-107G-E | 1000 | 1150 | Production Candidate |
| | | | 1.5 V/ 1.5 V | MT41J128M16JT-107G-E | 1000 | 1150 | Production Candidate |
| 256Mx16 DDR3 | Samsung | 0x3 | 1.5 V/ 1.5 V | K4V4G1646E-BC11 | 1000 | 1104 | Production Candidate |
| | | | 1.5 V/ 1.5 V | MT41J256M16H4-107G-E | 1000 | 1104 | Production Candidate |
| | Hynix | 0x1 | 1.5 V/ 1.5 V | MT41J256M16H4-107G-E | 1000 | 1104 | Production Candidate |
| | | | 1.5 V/ 1.5 V | MT41J256M16H4-107G-E | 1000 | 1104 | Production Candidate |

Table 8. N14P-GS/LP/GE/GT DDR3 Recommended Memories 128Mx16 Configuration

| Configuration | Vendor | Strap | FBVDD/ FBVDDQ | Manufacturer Part Number | Max Speed CK (MHz) | Memory Date Code Minimum | Status |
|---------------|---------|-------|------------------|-----------------------------|-----------------------------|--------------------------------|---------------------|
| 128Mx16 DDR3 | Samsung | 0x7 | 1.5 V/ 1.5 V | K4V2G1646E-BC11 | 1000 | 1204 | Production ready |
| | | | 1.5 V/ 1.5 V | MT41J128M16JT-107G-E | 1000 | 1204 | Production ready |
| | Hynix | 0x5 | 1.5 V/ 1.5 V | MT41J128M16JT-107G-E | 1000 | 1150 | Production ready |
| | | | 1.5 V/ 1.5 V | MT41J128M16JT-107G-E | 1000 | 1150 | Production ready |
| 256Mx16 DDR3 | Samsung | 0x3 | 1.5 V/ 1.5 V | K4V4G1646E-BC11 | 1000 | 1104 | Production ready |
| | | | 1.5 V/ 1.5 V | MT41J256M16H4-107G-E | 1000 | 1104 | Production ready |
| | Hynix | 0x1 | 1.5 V/ 1.5 V | MT41J256M16H4-107G-E | 1000 | 1104 | Production ready |
| | | | 1.5 V/ 1.5 V | MT41J256M16H4-107G-E | 1000 | 1104 | Production ready |

Table 2. N14M-GE/GL DDR3 Recommended Memories 256Mx16 Configuration

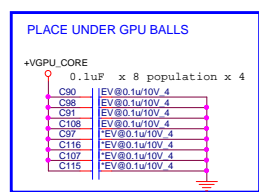
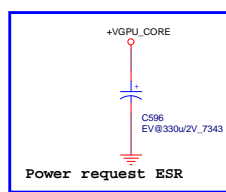
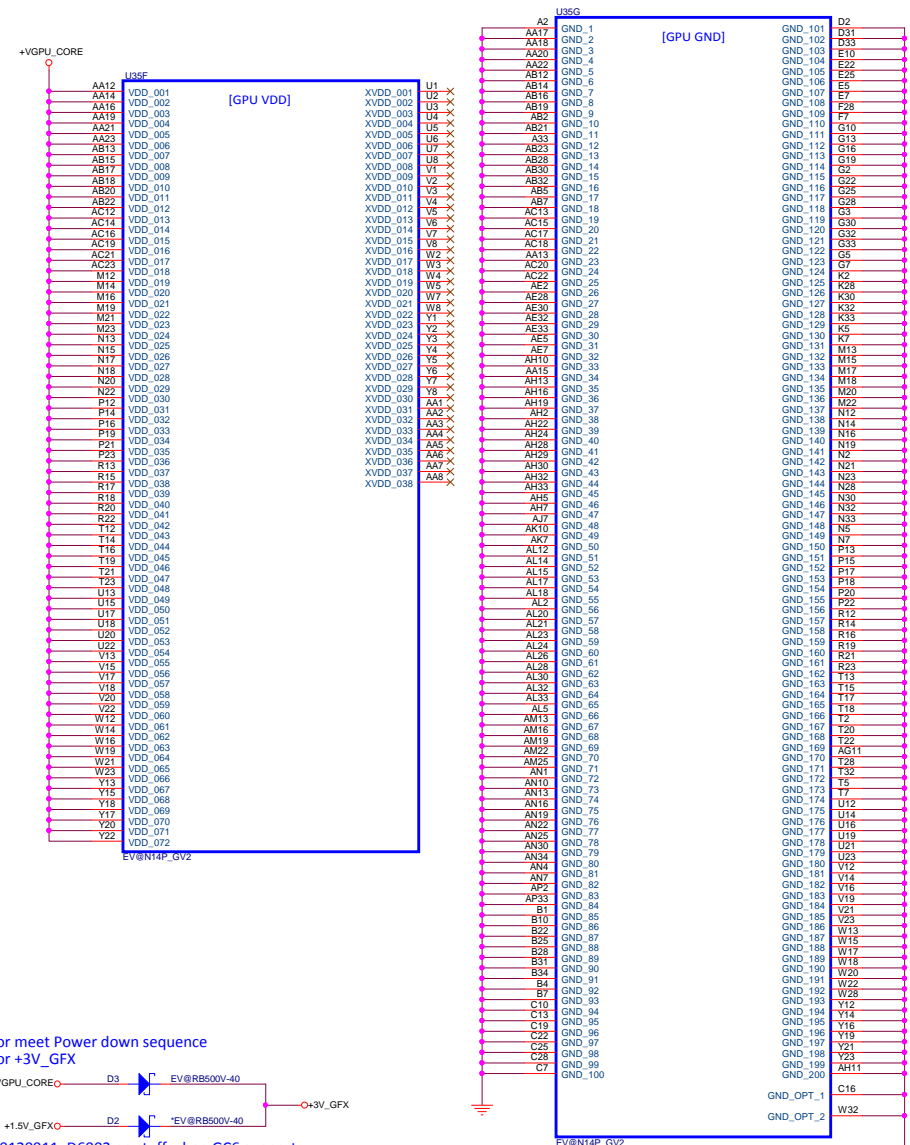
| Configuration | Vendor | Strap | FBVDD/ FBVDDQ | Manufacturer Part Number | Max Speed CK (MHz) | Memory Date Code Minimum | Status |
|---------------|---------|-------|------------------|-----------------------------|-----------------------------|--------------------------------|---------------------|
| 256Mx16 DDR3 | Samsung | 0x5 | 1.5 V/ 1.5 V | K4V4G1646E-BC11 | 1000 | 1104 | Production ready |
| | | | 1.5 V/ 1.5 V | MT41J256M16H4-107G-E | 1000 | 1104 | Production ready |
| | Hynix | 0x1 | 1.5 V/ 1.5 V | MT41J256M16H4-107G-E | 1000 | 1104 | Production ready |
| | | | 1.5 V/ 1.5 V | MT41J256M16H4-107G-E | 1000 | 1104 | Production ready |

Table 1. N14M-GE/GL DDR3 Recommended Memories 128Mx16 Configuration

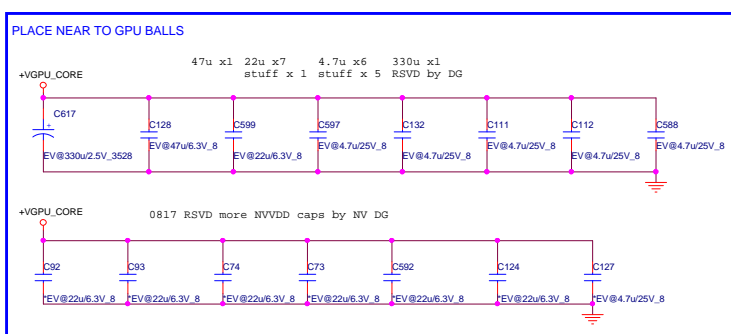
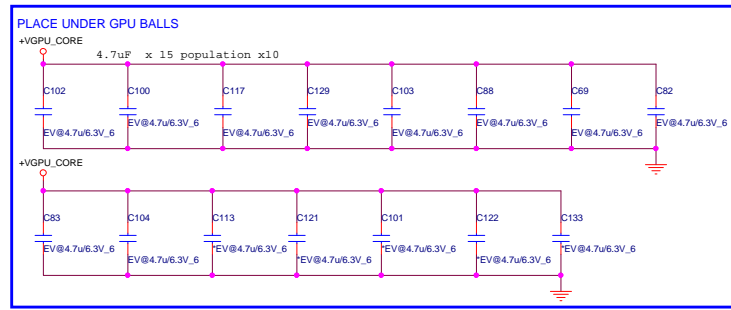
| Configuration | Vendor | Strap | FBVDD/ FBVDDQ | Manufacturer Part Number | Max Speed CK (MHz) | Memory Date Code Minimum | Status |
|---------------|---------|-------|------------------|-----------------------------|-----------------------------|--------------------------------|---------------------|
| 128Mx16 DDR3 | Samsung | 0x7 | 1.5 V/ 1.5 V | K4V2G1646E-BC11 | 1000 | 1204 | Production ready |
| | | | 1.5 V/ 1.5 V | MT41J128M16JT-107G-E | 1000 | 1204 | Production ready |
| | Hynix | 0x5 | 1.5 V/ 1.5 V | MT41J128M16JT-107G-E | 1000 | 1150 | Production ready |
| | | | 1.5 V/ 1.5 V | MT41J128M16JT-107G-E | 1000 | 1150 | Production ready |
| 256Mx16 DDR3 | Samsung | 0x3 | 1.5 V/ 1.5 V | K4V4G1646E-BC11 | 1000 | 1104 | Production ready |
| | | | 1.5 V/ 1.5 V | MT41J256M16H4-107G-E | 1000 | 1104 | Production ready |
| | Hynix | 0x1 | 1.5 V/ 1.5 V | MT41J256M16H4-107G-E | 1000 | 1104 | Production ready |
| | | | 1.5 V/ 1.5 V | MT41J256M16H4-107G-E | 1000 | 1104 | Production ready |

| Vendor | Strap | Q PN | Mem. PN | Freq. | GPU |
|--------|-------|-------------|----------------------|--------|----------------|
| Micron | 0001 | AKD5PGSTL05 | MT41K256M16HA-107G:E | 900MHz | N14P-GT1 & GV2 |
| Bynlix | 0110 | AKD5MGTW17 | H5TQ2G63DR-11C | 900MHz | N14P-GT |

| | | | |
|---|-----------------|----------------------|--|
|  | | Quanta Computer Inc. | |
| | | PROJECT : ZGK | |
| Doc | Document Number | DGPU 4/5 (MIO/GPIO) | |
| Rev | Version | Rev 1A | |



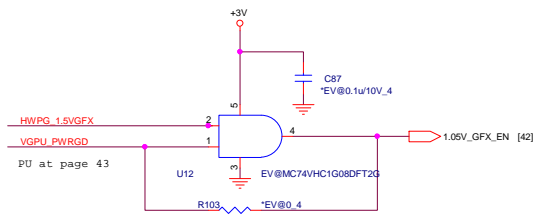
LAYOUT NOTES:
UNDAER: WITHIN 150MILS
NEAR: WITHIN 1378MILS



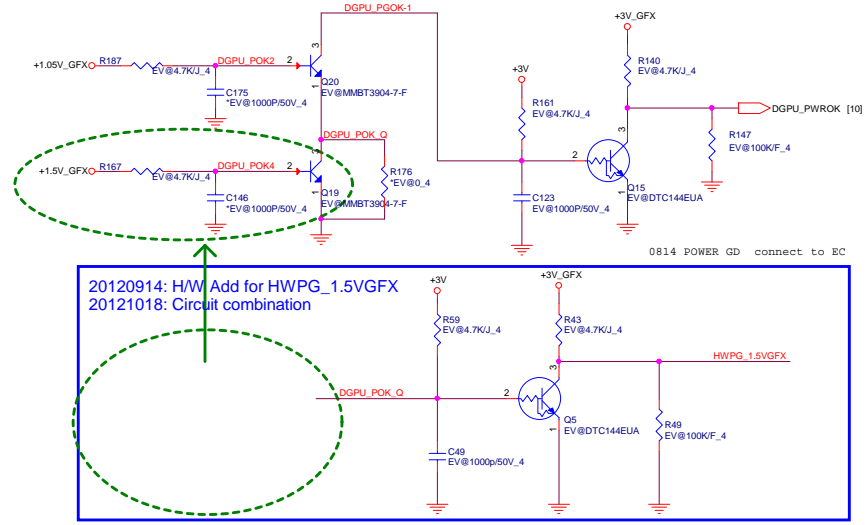
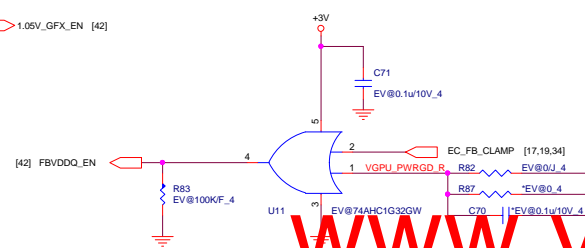
for meet Power down sequence for +3V GFX



20120911: D6002 no stuff when GC6 support.



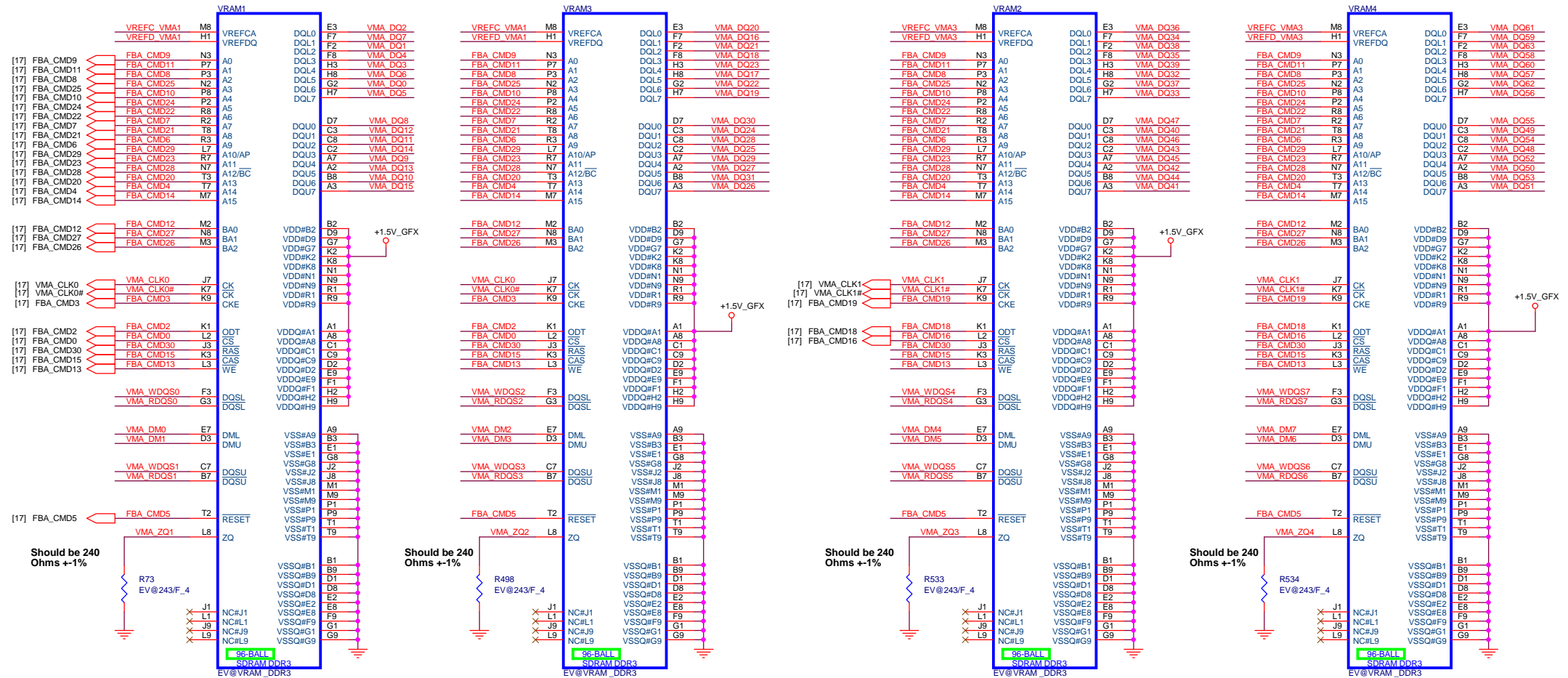
0816 GC6 need system 3V to control FBVDDQ



20120914: H/W Add for HWPG_1.5VGFX
2012018: Circuit combination

[17] VMA_DQ[63..0]
[17] VMA_DM[7..0]
[17] VMA_WDQS[7..0]
[17] VMA_RDQS[7..0]

CHANNEL A: 1024MB DDR3

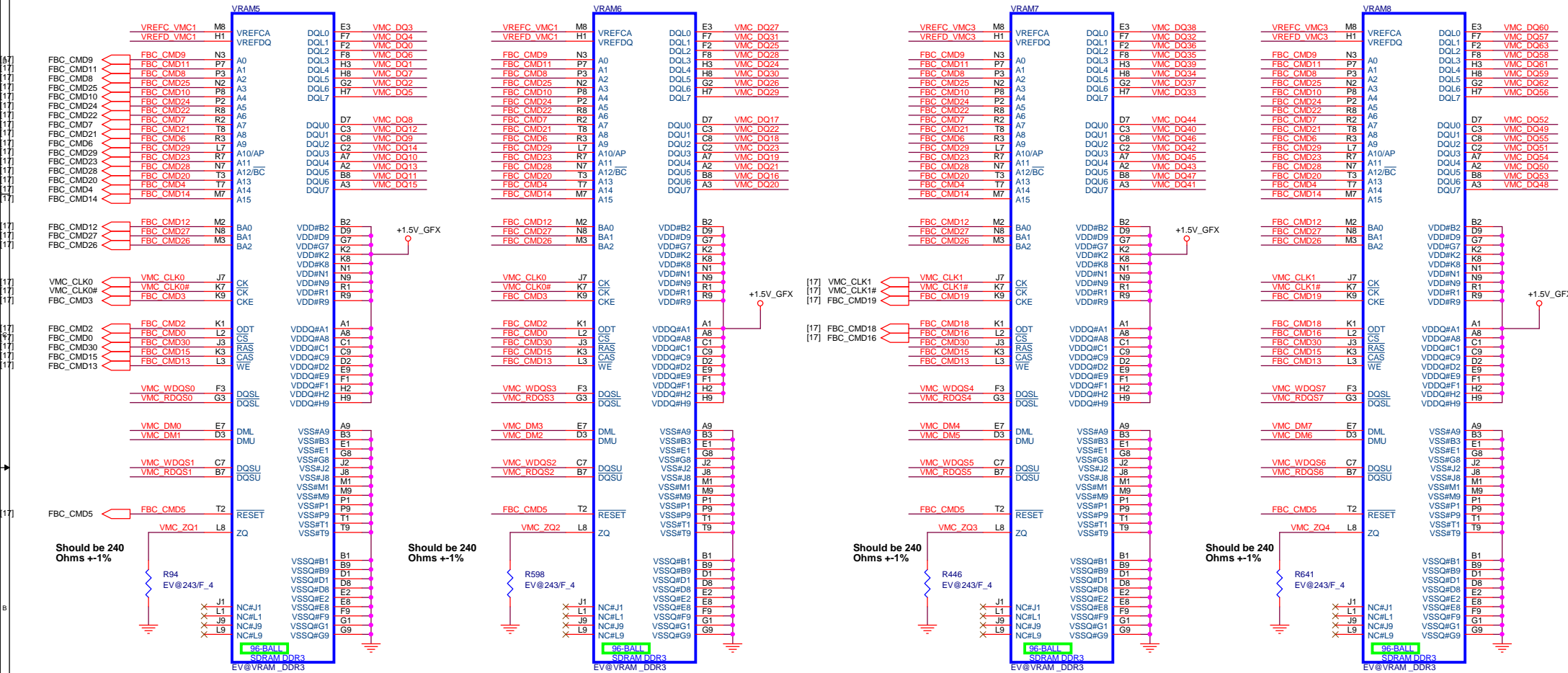


Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W $\pm 5\%$ (0402)
2 : CS11622PB07 ,RES CHIP 162 1/16W $\pm 1\%$ (0402)

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W $\pm 5\%$ (0402)
2 : CS11622PB07 ,RES CHIP 162 1/16W $\pm 1\%$ (0402)

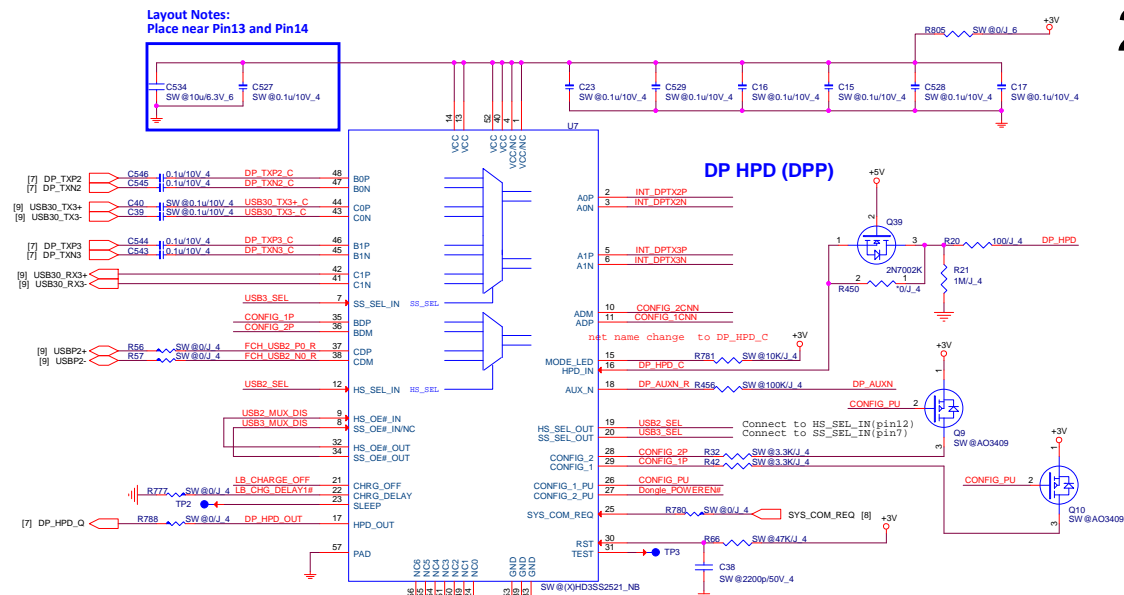
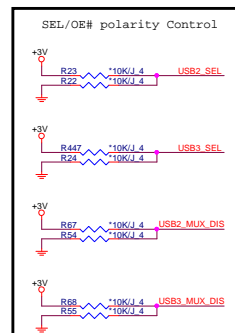
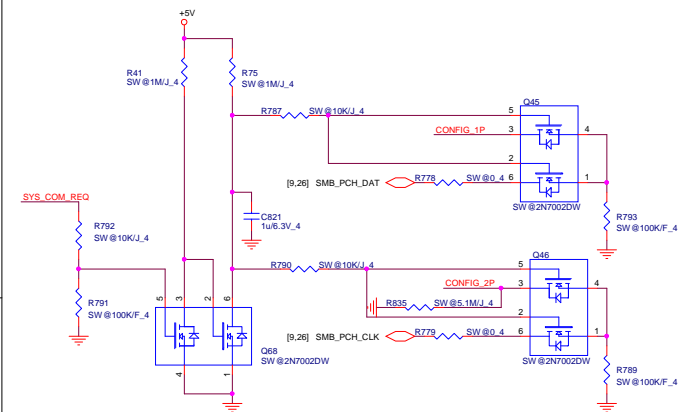
[17] VMC_DQ[63..0]
[17] VMC_DM[7..0]
[17] VMC_WDQS[7..0]
[17] VMC_RDQS[7..0]

CHANNEL B: 1024MB DDR3

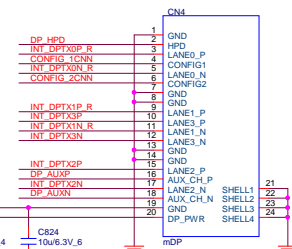


Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

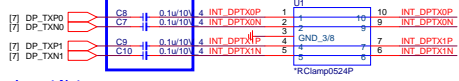
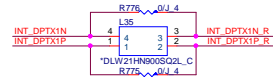
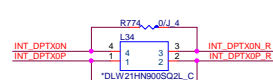
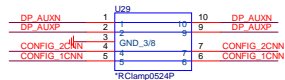
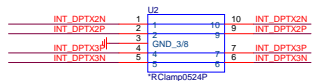
Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)



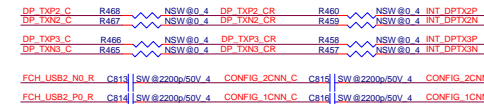
MINI DP connector (DPP)



ESD Protect (EMC)

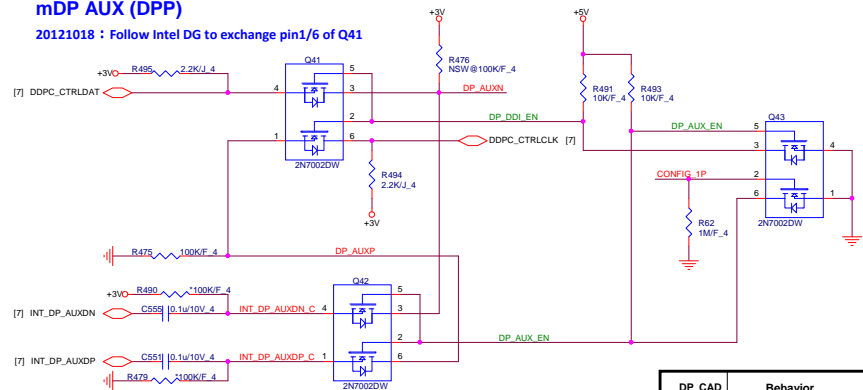


Layout Notes:
Place decoupling CAPs close to Connector

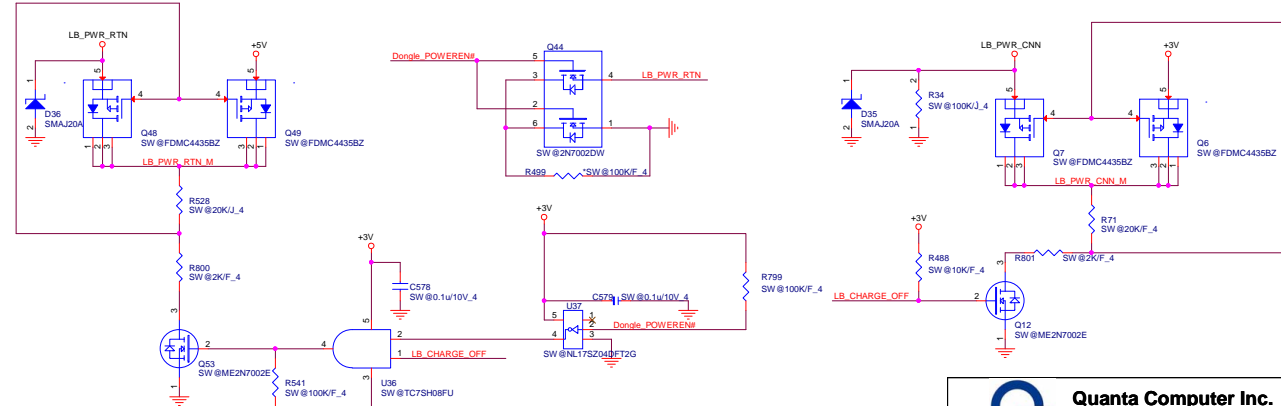


mDP AUX (DPP)

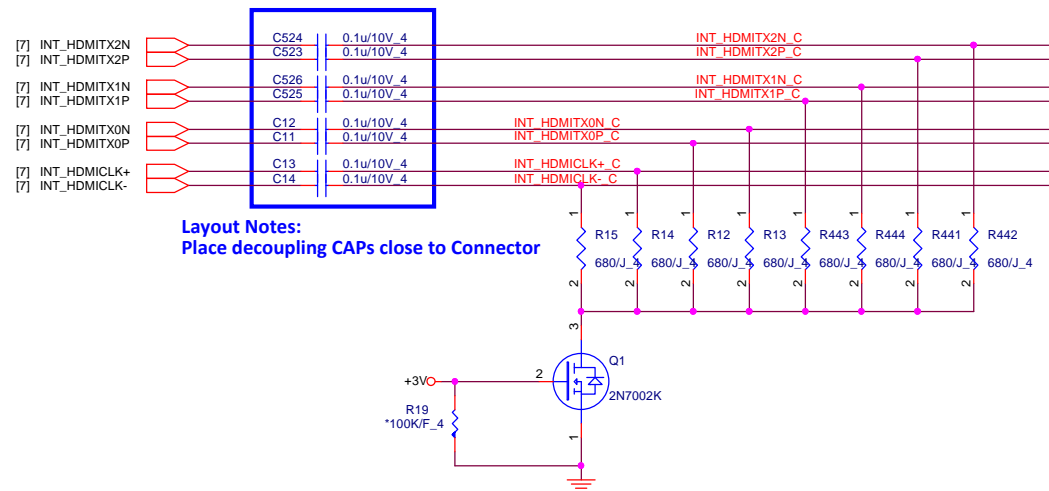
20121018 : Follow Intel DG to exchange pin1/6 of Q41



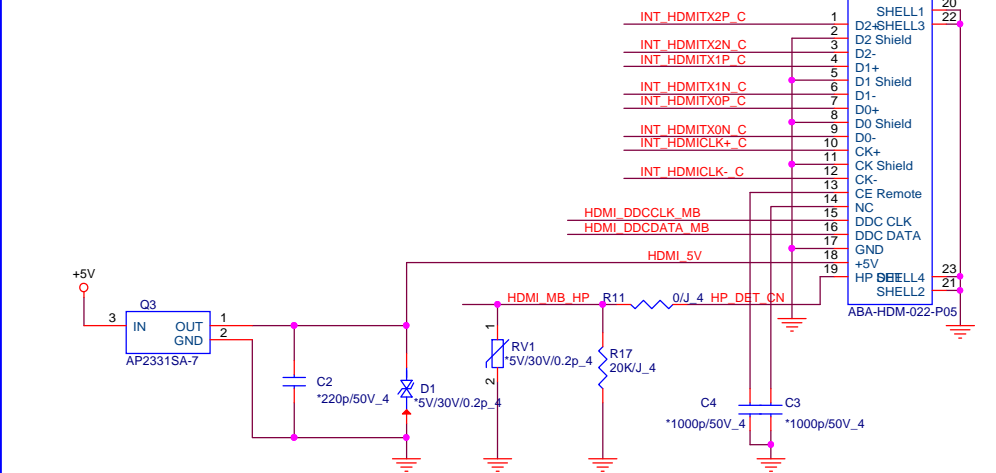
| DP_CAD | Behavior |
|--------|-------------------------|
| Low | DP signal (AC couple) |
| High | TMDS signal (DC couple) |



HDMI Cost Reduced level shift (HDM)

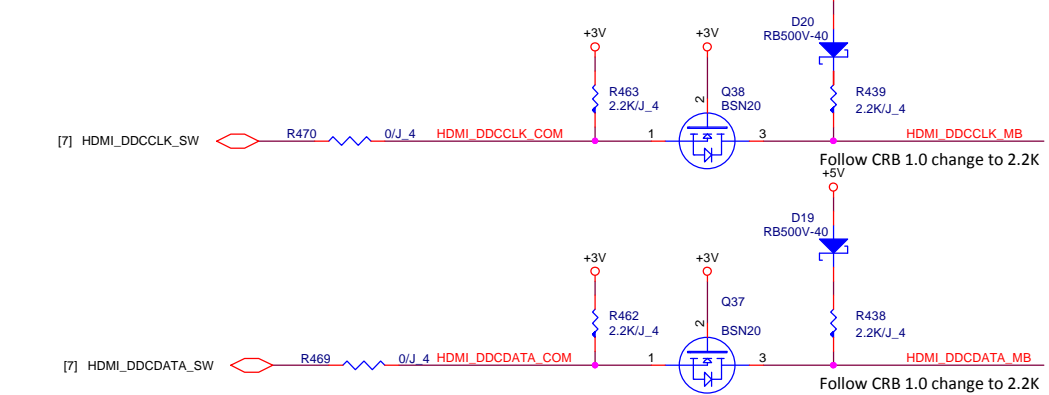


HDMI connector (HDM)

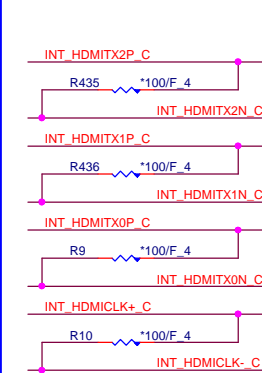


25

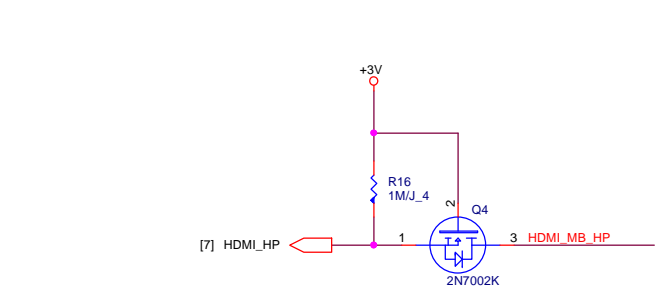
HDMI DDC (HDM)




EMI (EMC)

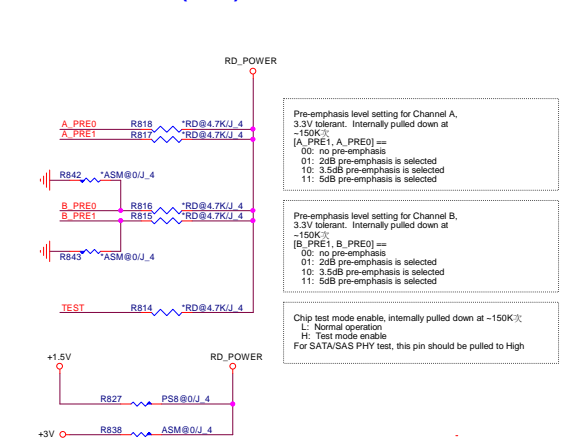


HDMI-detect (HDM)

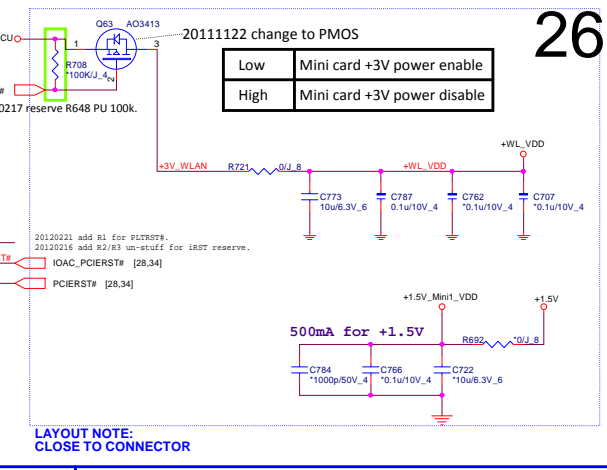
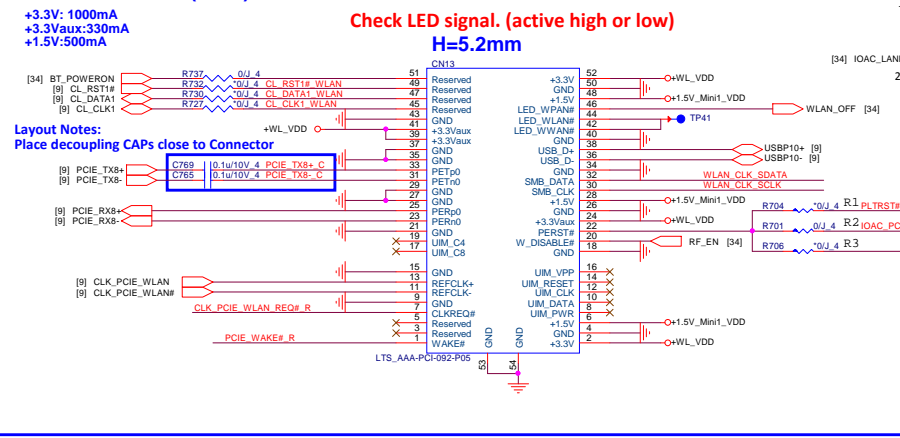


| | | |
|--|-----------------------|-------------------------|
|  Quanta Computer Inc. PROJECT : ZQK | | Rev 1A |
| | | |
| Date: Monday, January 07, 2013 | Sheet 25 of 46 | Rev 1A |

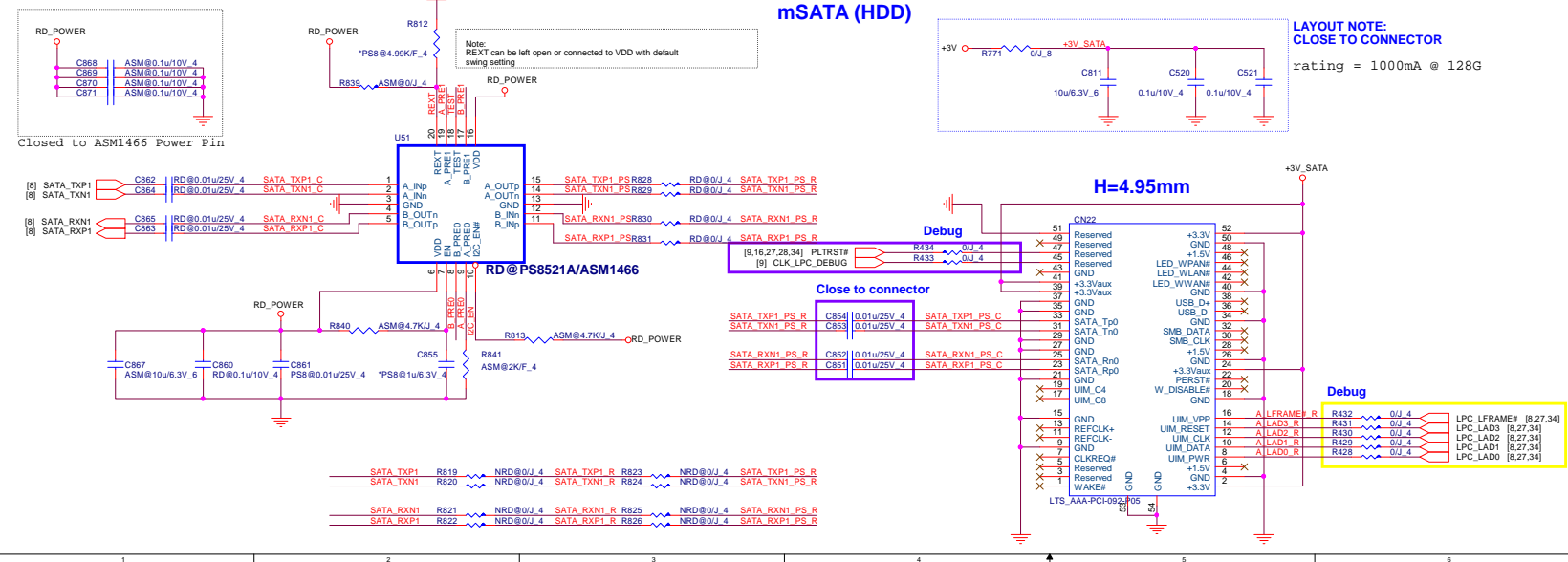
mSATA Redriver (HDD)



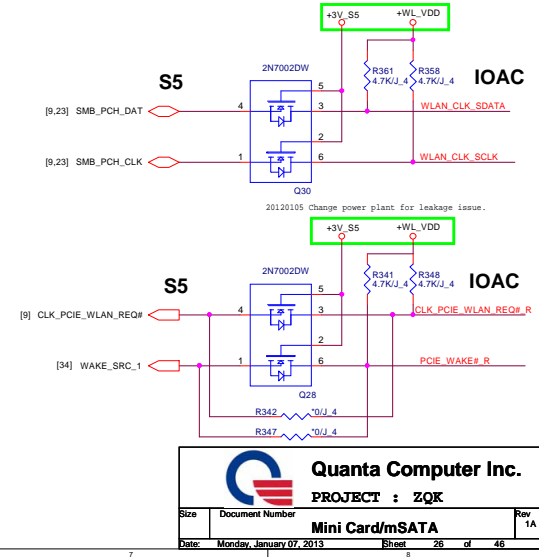
MINI-CARD WLAN(MPC)



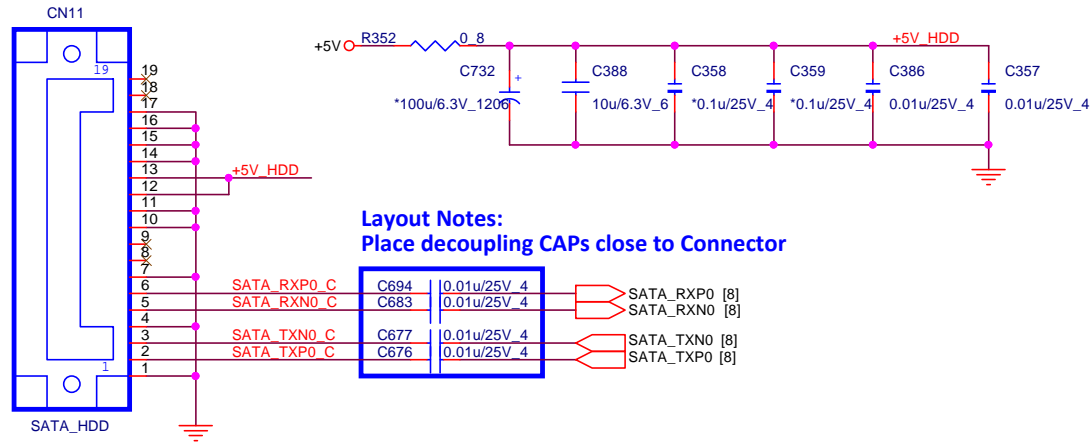
mSATA (HDD)



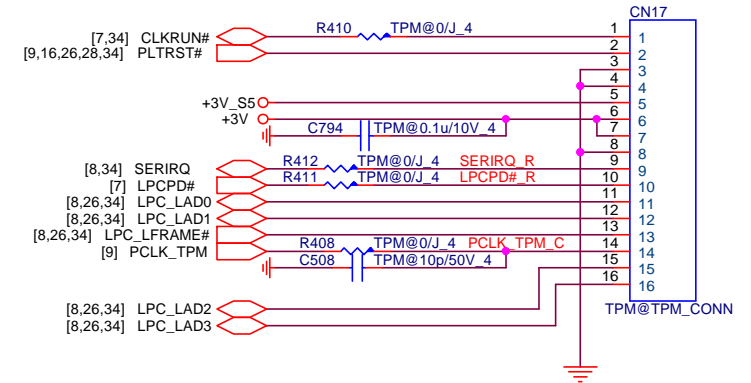
Leakage circuit (MPC)



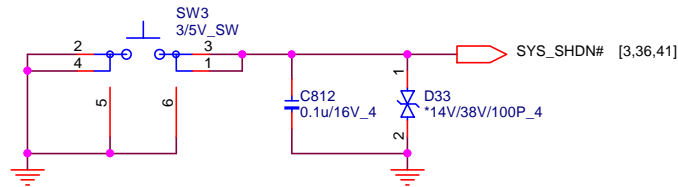
MAIN SATA HDD (HDD)



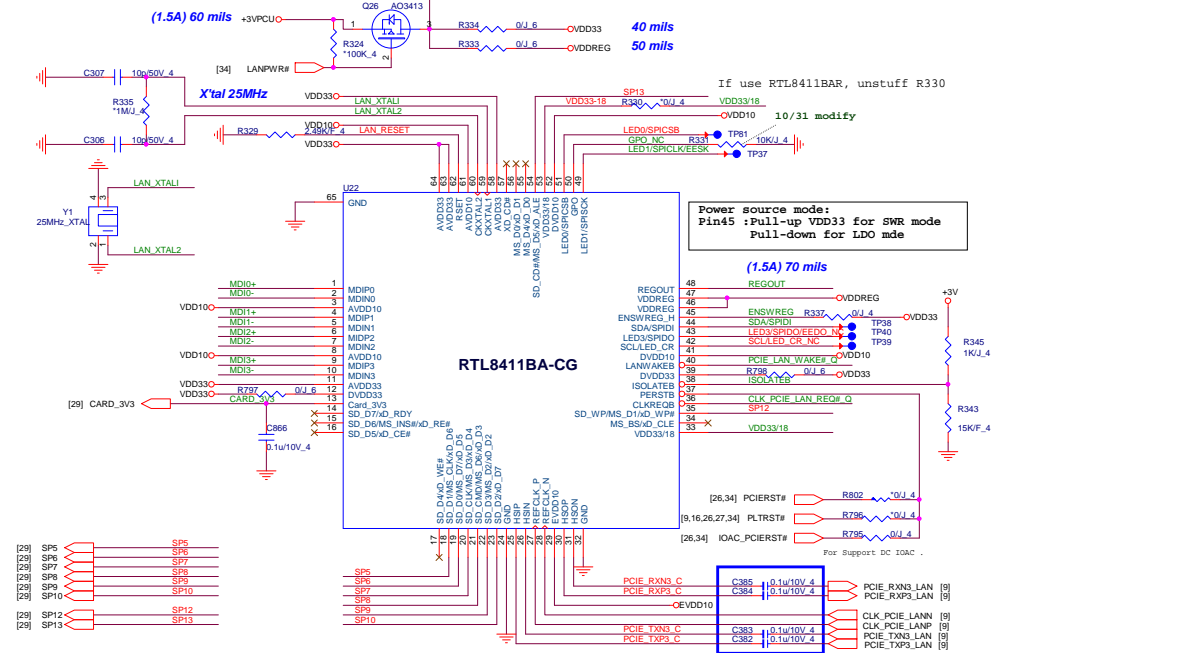
TPM (TPM)



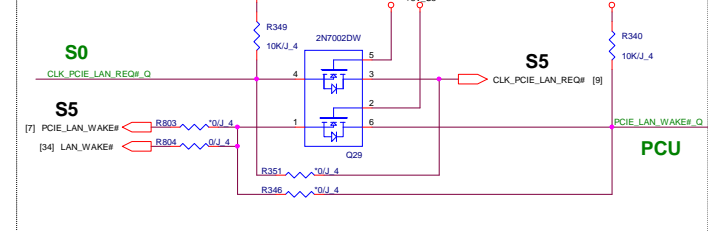
3/5VPCU reset switch (CLG)



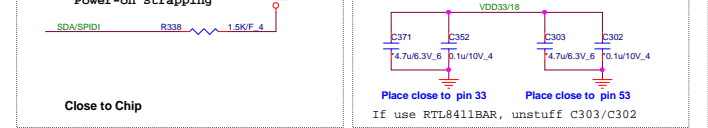
LAN/Card reader (LAN)



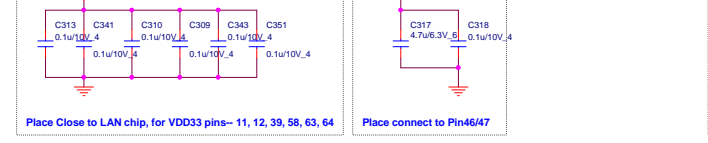
Leakage circuit (LAN)



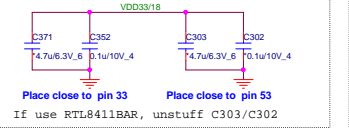
Power-on Strapping



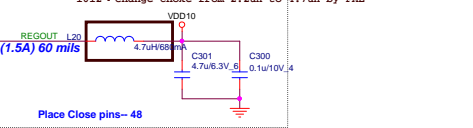
Max current is 1400mA keep routing trace at least 50 mil



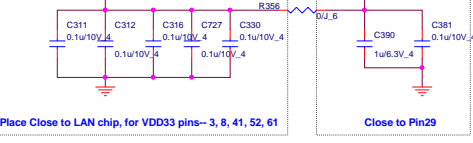
10 mils



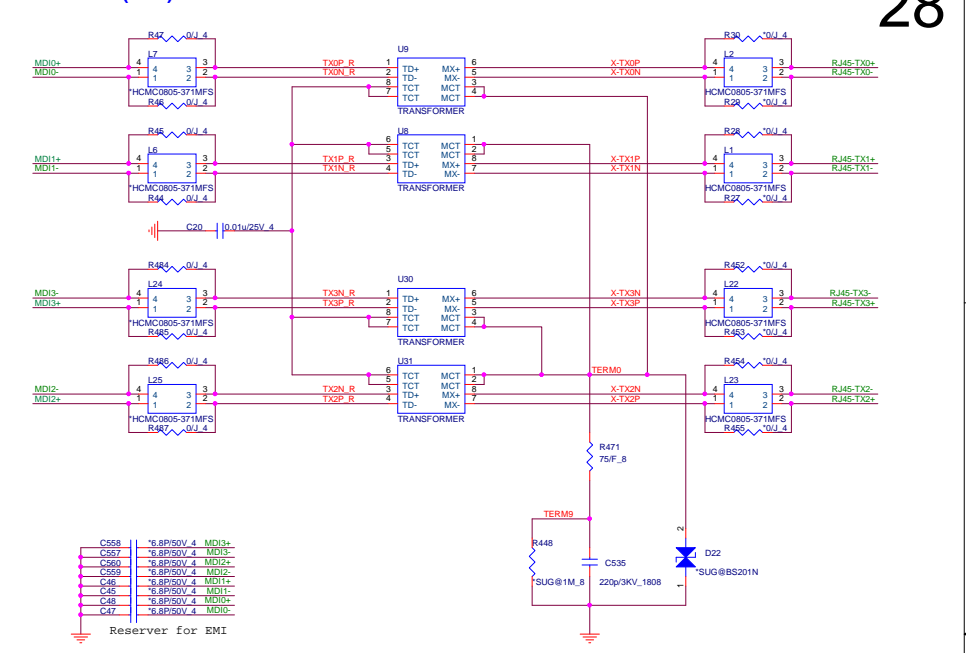
1012 : Change choke from 2.2uH to 4.7uH by FAE



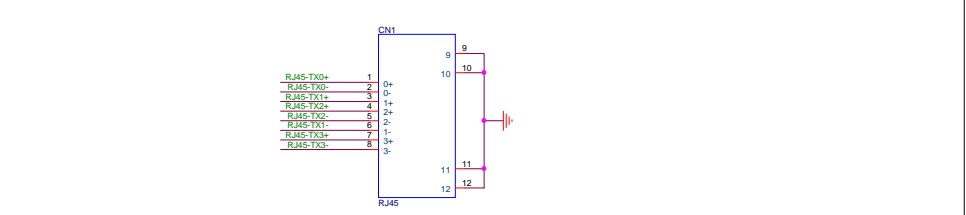
(1.5A) 60 mils



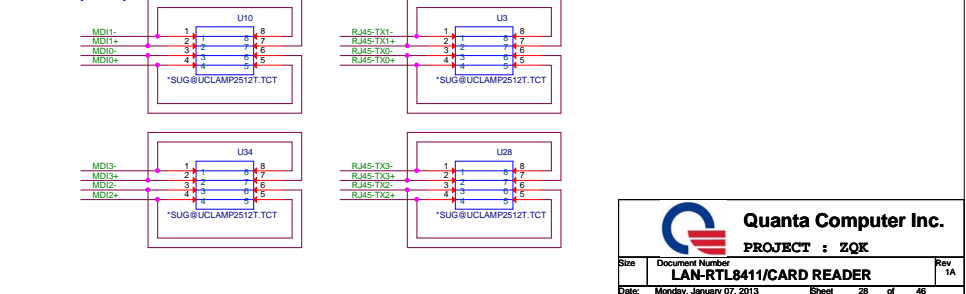
Transformer (LAN)



RJ45 CONNECTOR (LAN)



SURGE (LAN)

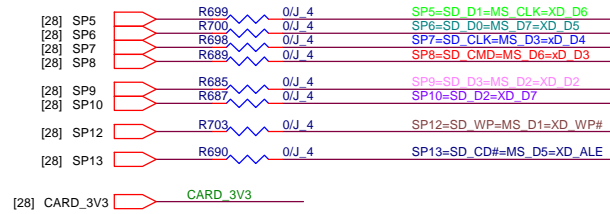
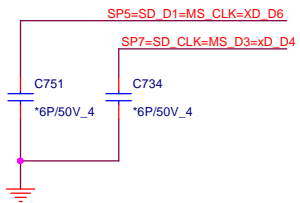


CARD READER CONNECTOR (MMC)

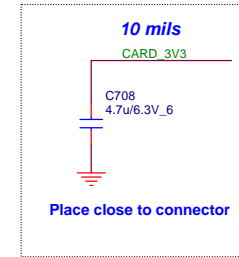
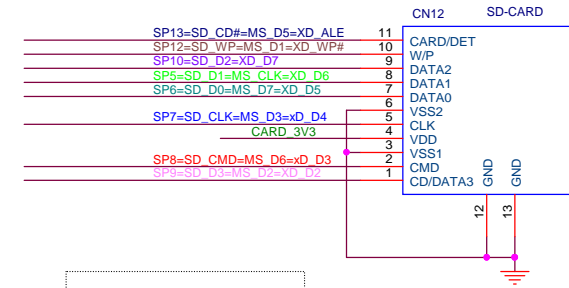
Share Pin

| | | | | |
|------|--------|---------|--|--------|
| SP1 | SD D7 | | | xD RDY |
| SP2 | SD D6 | MS INS# | | xD RE# |
| SP3 | SD D5 | | | xD CE# |
| SP4 | SD D4 | | | xD WE# |
| SP5 | SD D1 | MS CLK | | xD D6 |
| SP6 | SD D0 | MS D7 | | xD D5 |
| SP7 | SD CLK | MS D3 | | xD D4 |
| SP8 | SD CMD | MS D6 | | xD D3 |
| SP9 | SD D3 | MS D2 | | xD D2 |
| SP10 | SD D2 | | | xD D7 |
| SP11 | | MS BS | | xD CLE |
| SP12 | SD WP | MS D1 | | xD WP# |
| SP13 | SD CD# | MS D5 | | xD ALE |
| SP14 | | MS D4 | | xD D0 |
| SP15 | | MS D0 | | xD D1 |
| SP16 | | | | xD CD# |

EMI

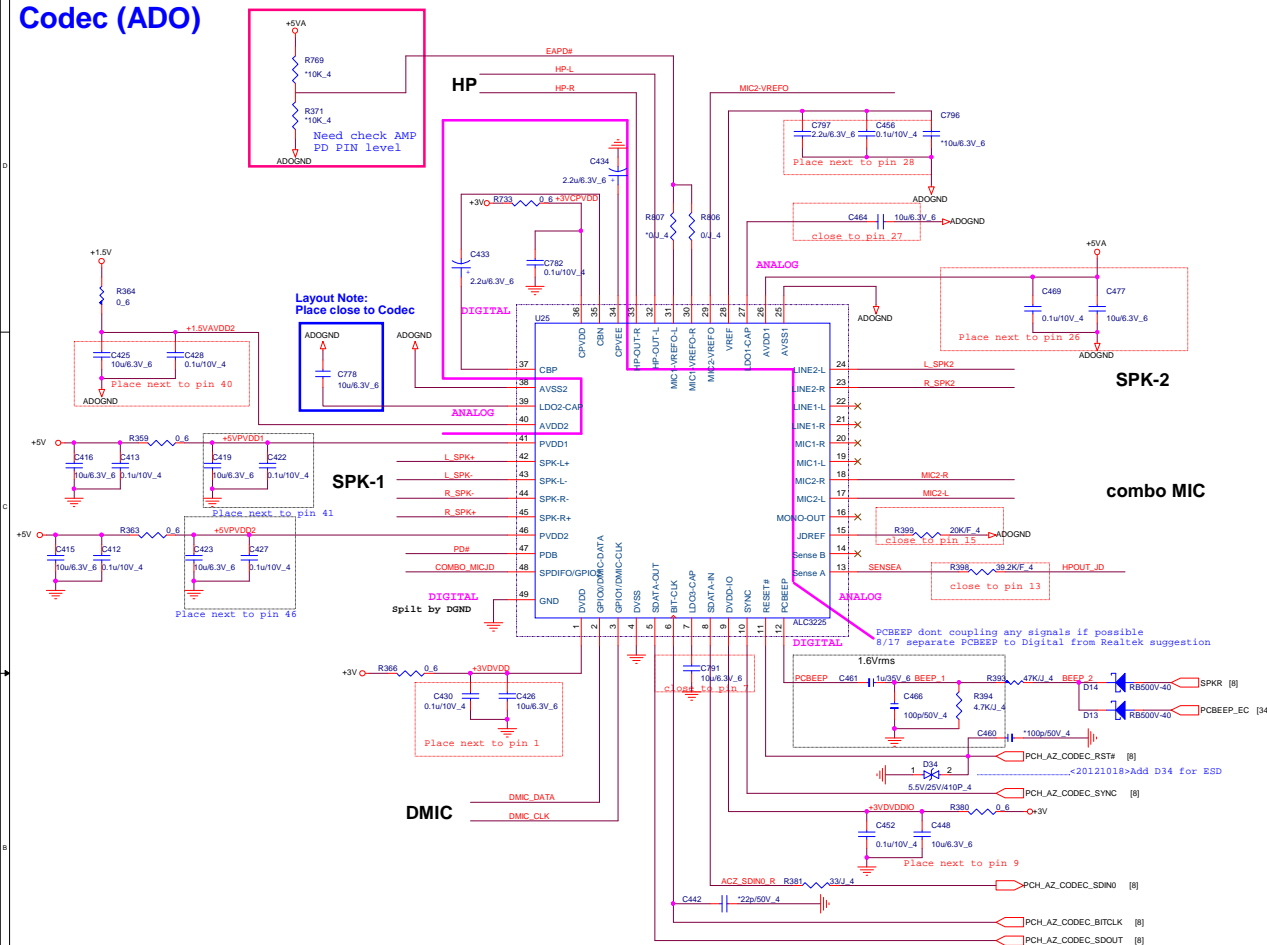


SD/MMC CARD READER (MMC)

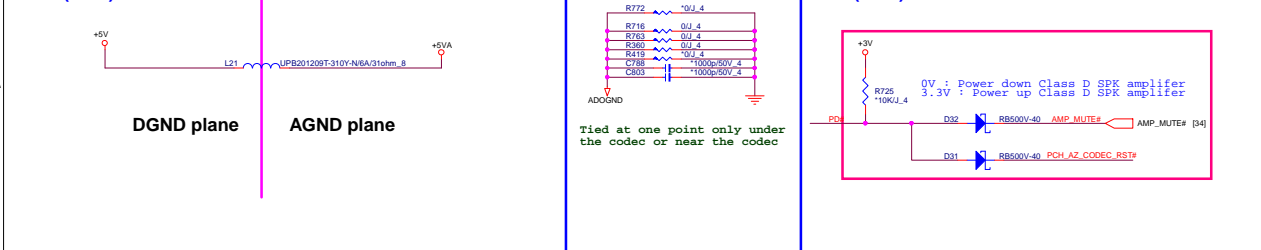


29

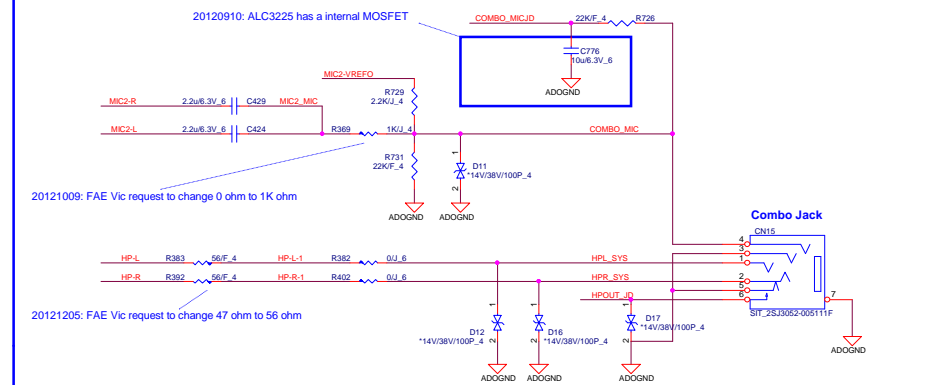
Codec (ADO)



Power(ADO)



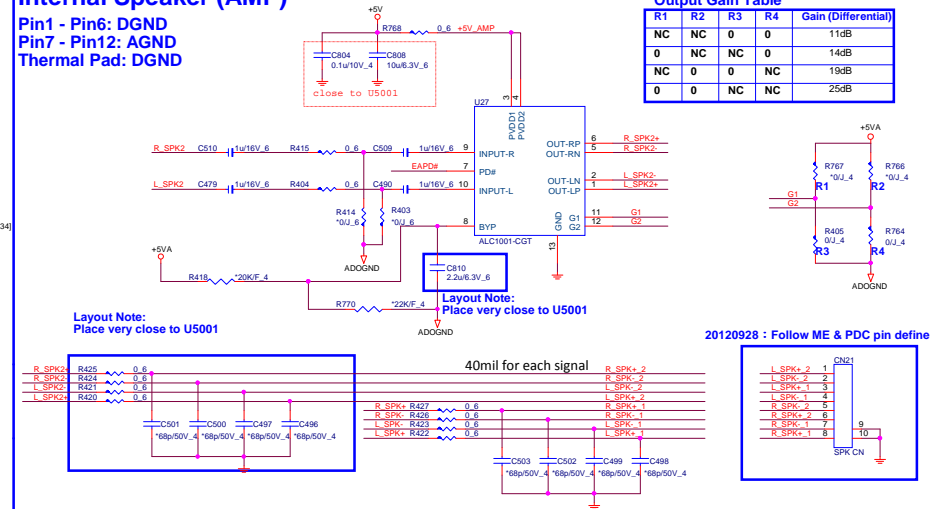
HEADPHONE/Mic combo (AMP)



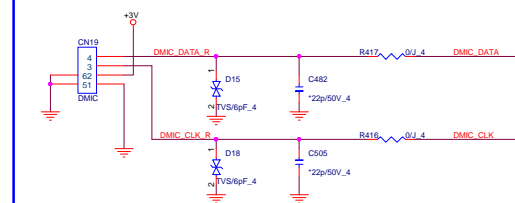
Internal Speaker (AMP)

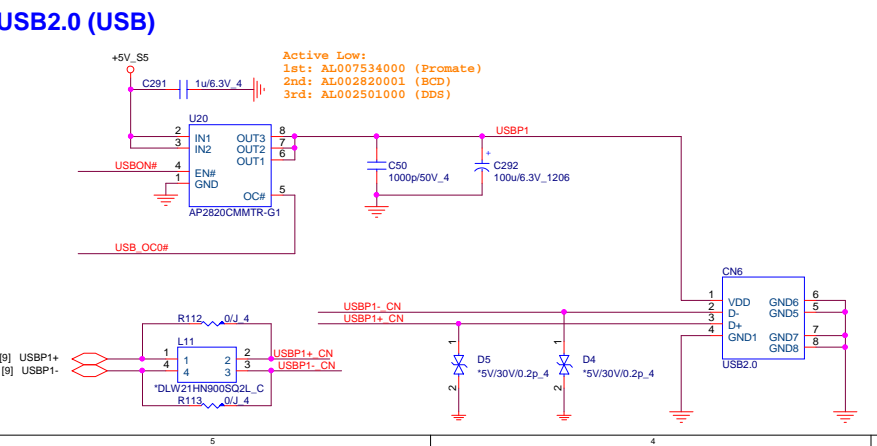
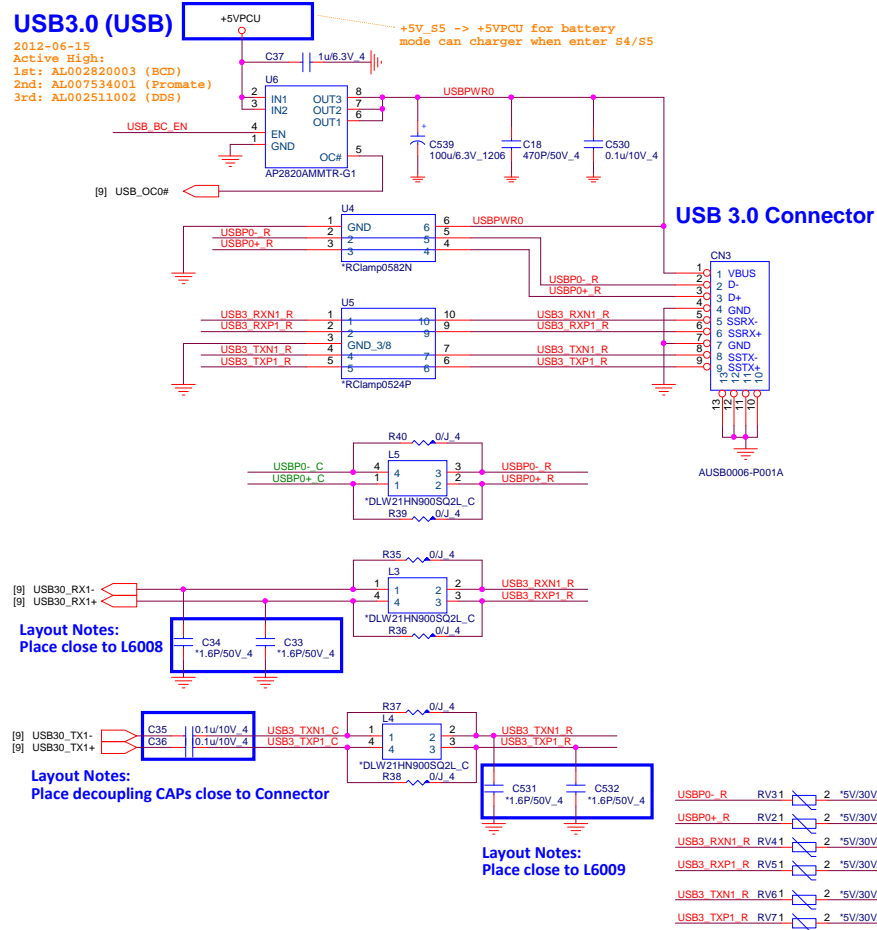
Pin1 - Pin6: DGND
Pin7 - Pin12: AGND
Thermal Pad: DGND

| R1 | R2 | R3 | R4 | Gain (Differential) |
|----|----|----|----|---------------------|
| NC | NC | 0 | 0 | 11dB |
| 0 | NC | NC | 0 | 14dB |
| NC | 0 | 0 | NC | 19dB |
| 0 | 0 | NC | NC | 25dB |



INT DMIC (AMP)

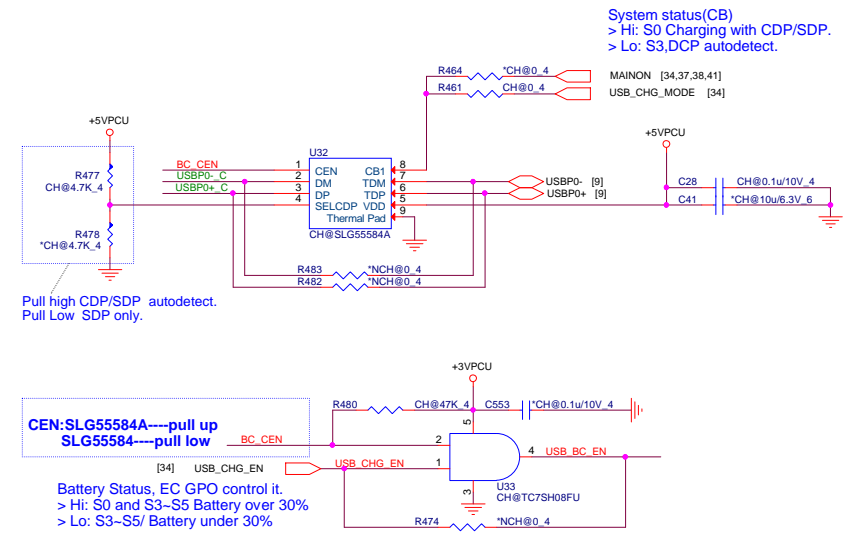




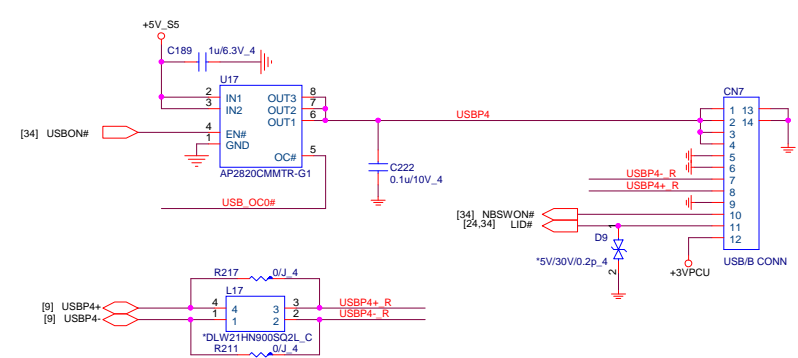
USB Charger to 3.0 (USB)


| Name | USB data | State | Max Current | Apple Device |
|----------|----------|-------|-------------|--------------|
| SDP | YES | S0-S3 | 500mA | 500mA |
| CDP | YES | S0-S3 | 1500mA | 500mA |
| DCP,Auto | NO | S4-S5 | 1800mA | 1800mA |

CH@: Default stuff



I/O board (USB)

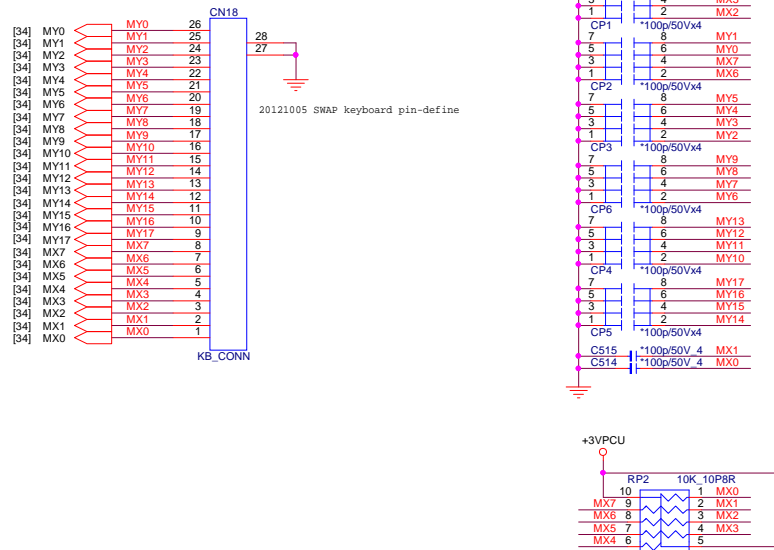




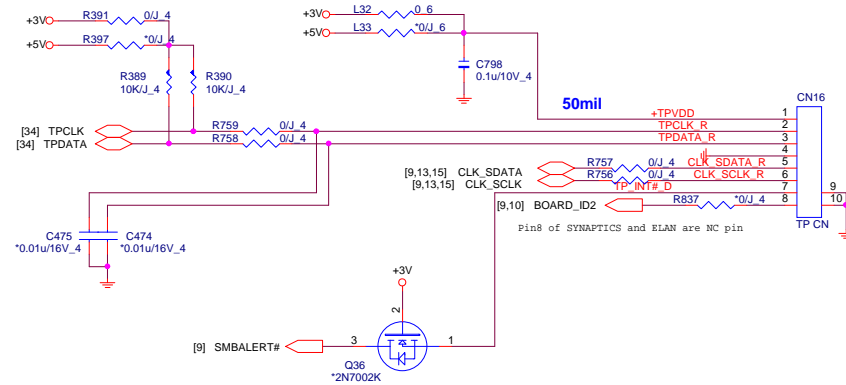
Quanta Computer Inc.
PROJECT : ZQK

| | | |
|-------|--------------------------|----------------|
| Size | Document Number | Rev |
| | INT&EXT USB | 1A |
| Date: | Monday, January 07, 2013 | Sheet 31 of 46 |

K/B (KBC)

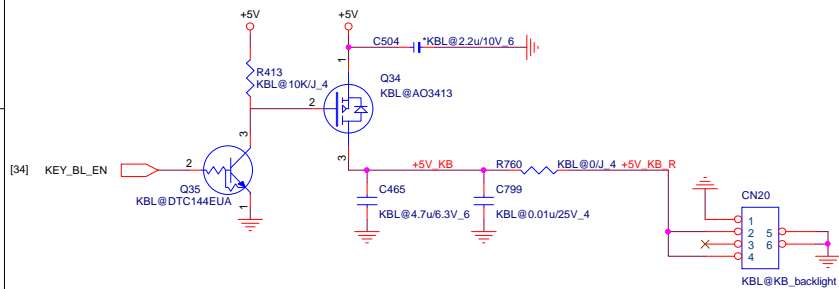


TOUCHPAD BOARD CONN (TPD)

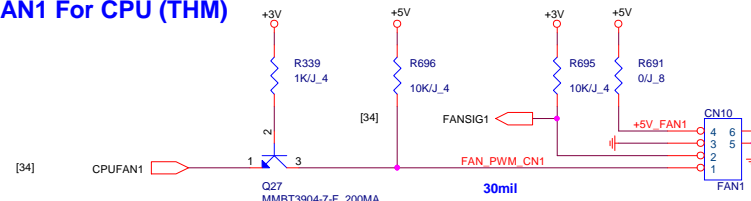


32

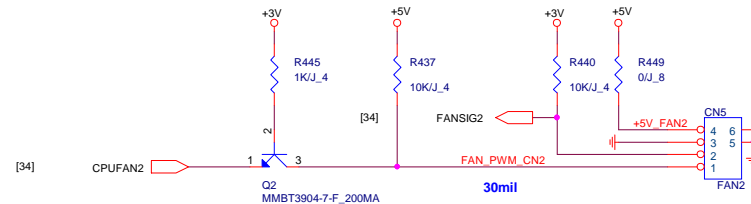
KB_BL LED (KBC)



FAN1 For CPU (THM)

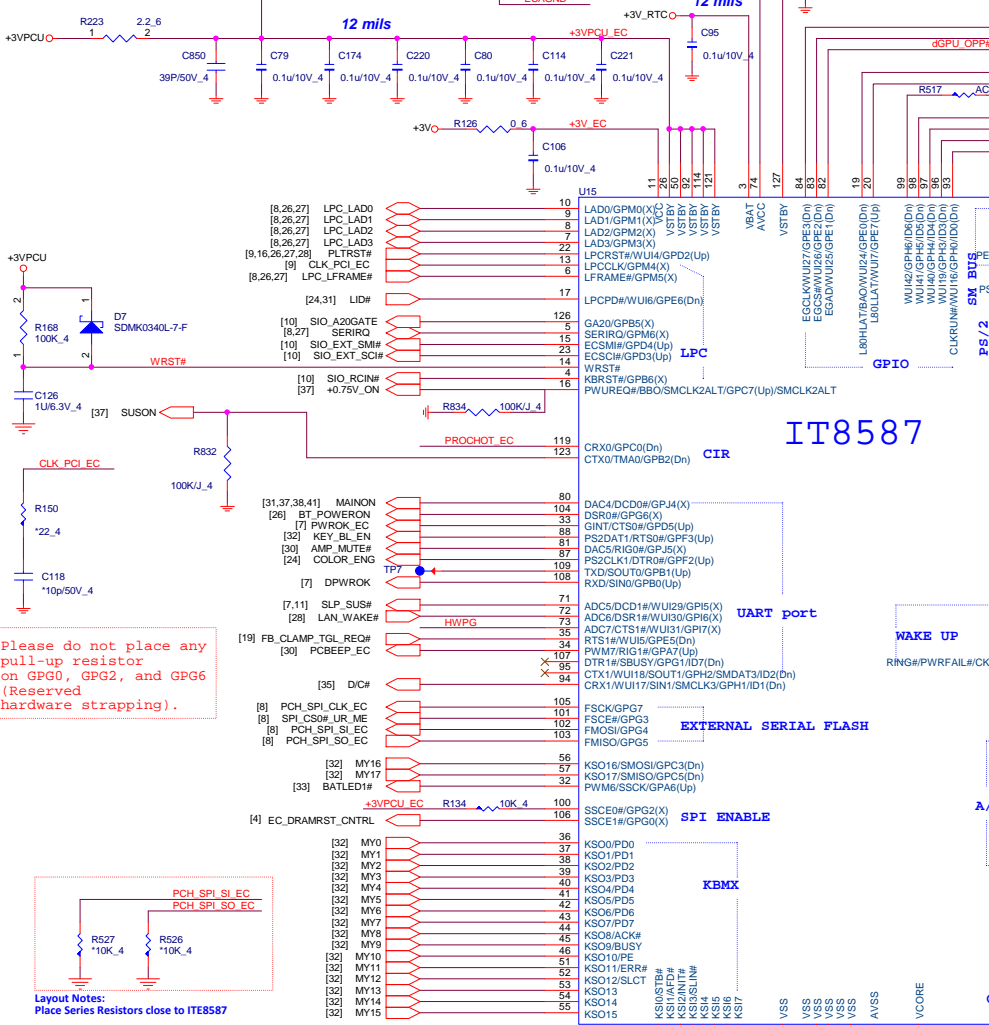


FAN2 For GPU (THM)



EC(KBC)

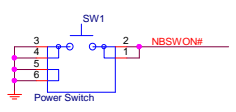
+3VPCU_EC and +3V_RTC
minimum trace width 12mils.



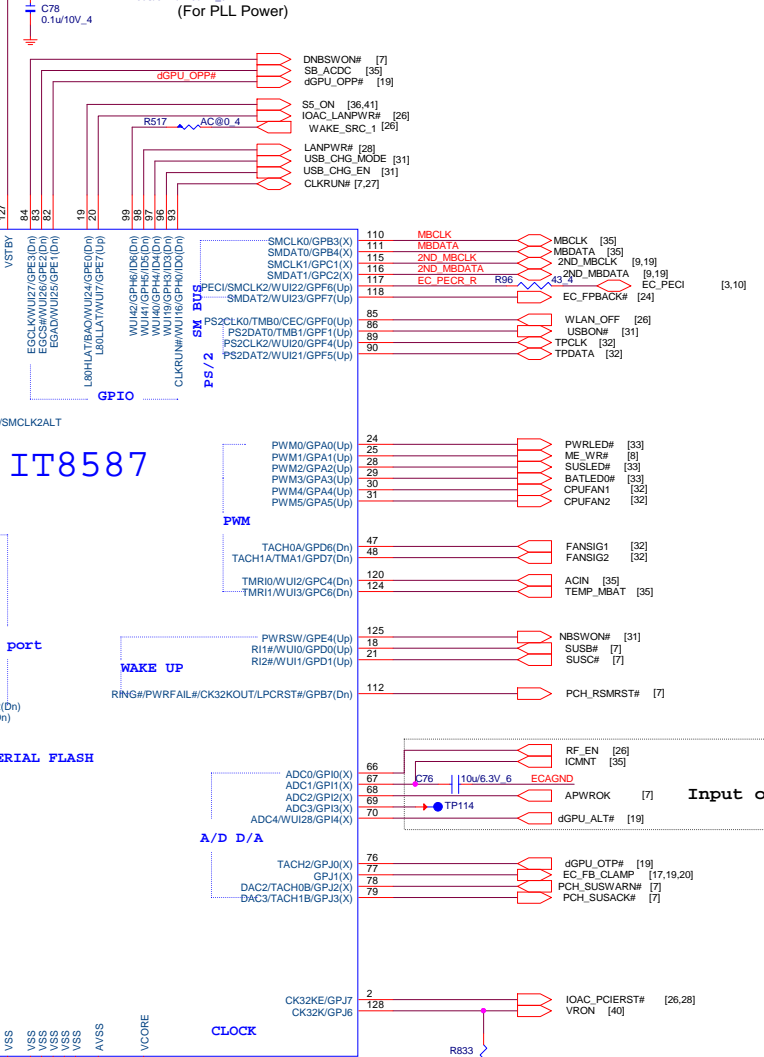
Please do not place any pull-up resistor on GP00, GP02, and GP06 (Reserved hardware strapping).

Layout Notes:
Place Series Resistors close to IT8587

For test only



1008 : Change Power rail from +3VPCU to +3VPCU_EC (For PLL Power)

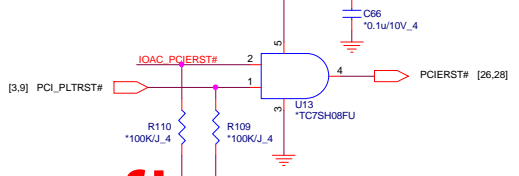


SM BUS ARRANGEMENT TABLE

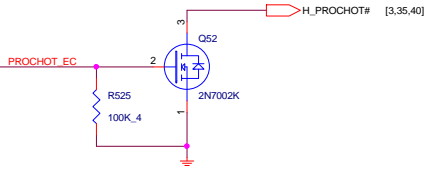
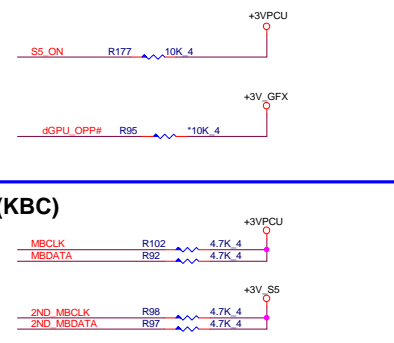
| | |
|----------|---------|
| SM Bus 1 | Battery |
| SM Bus 2 | PCH/VGA |

iRST

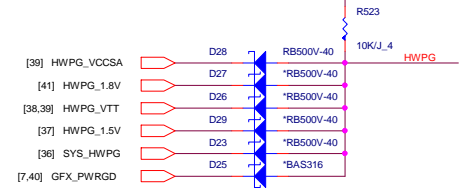
20120217 reserve iRST function.

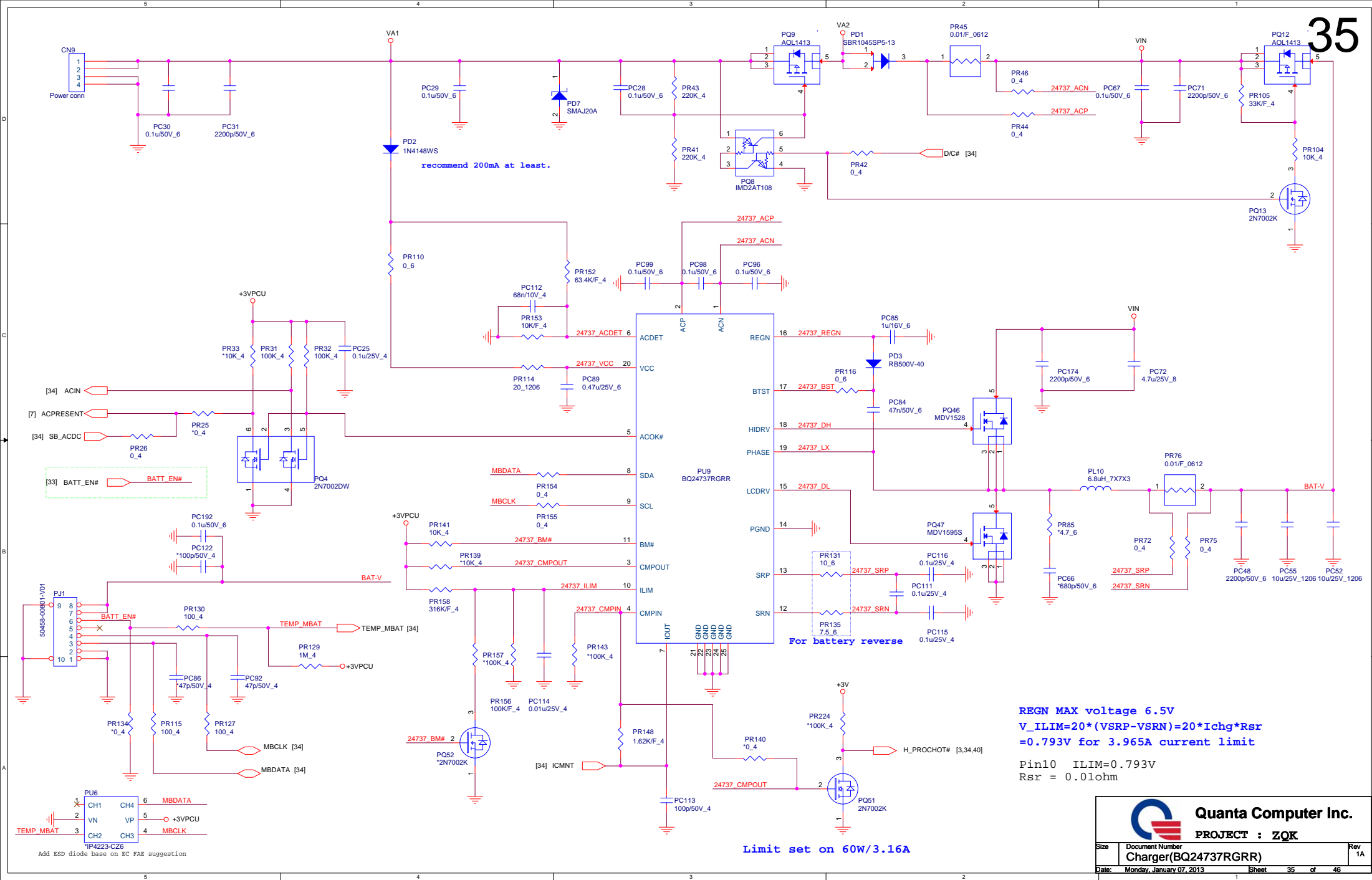



SM BUS PU(KBC)

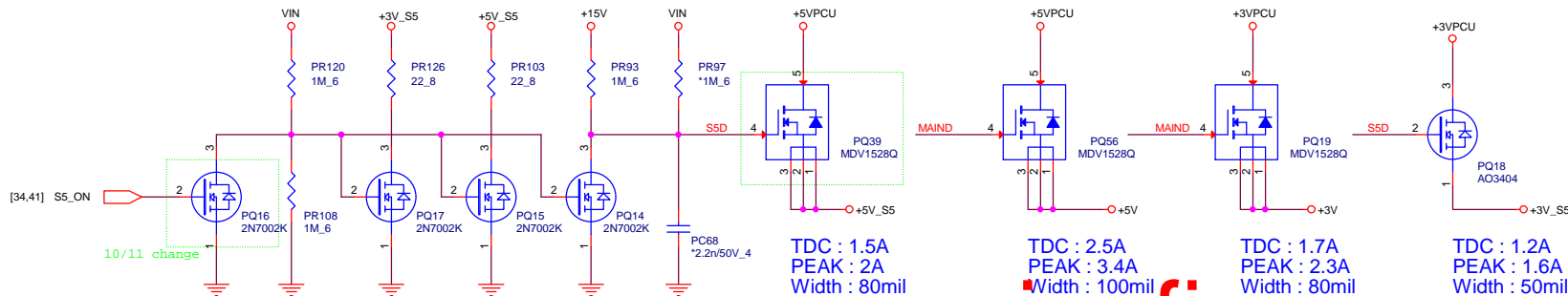
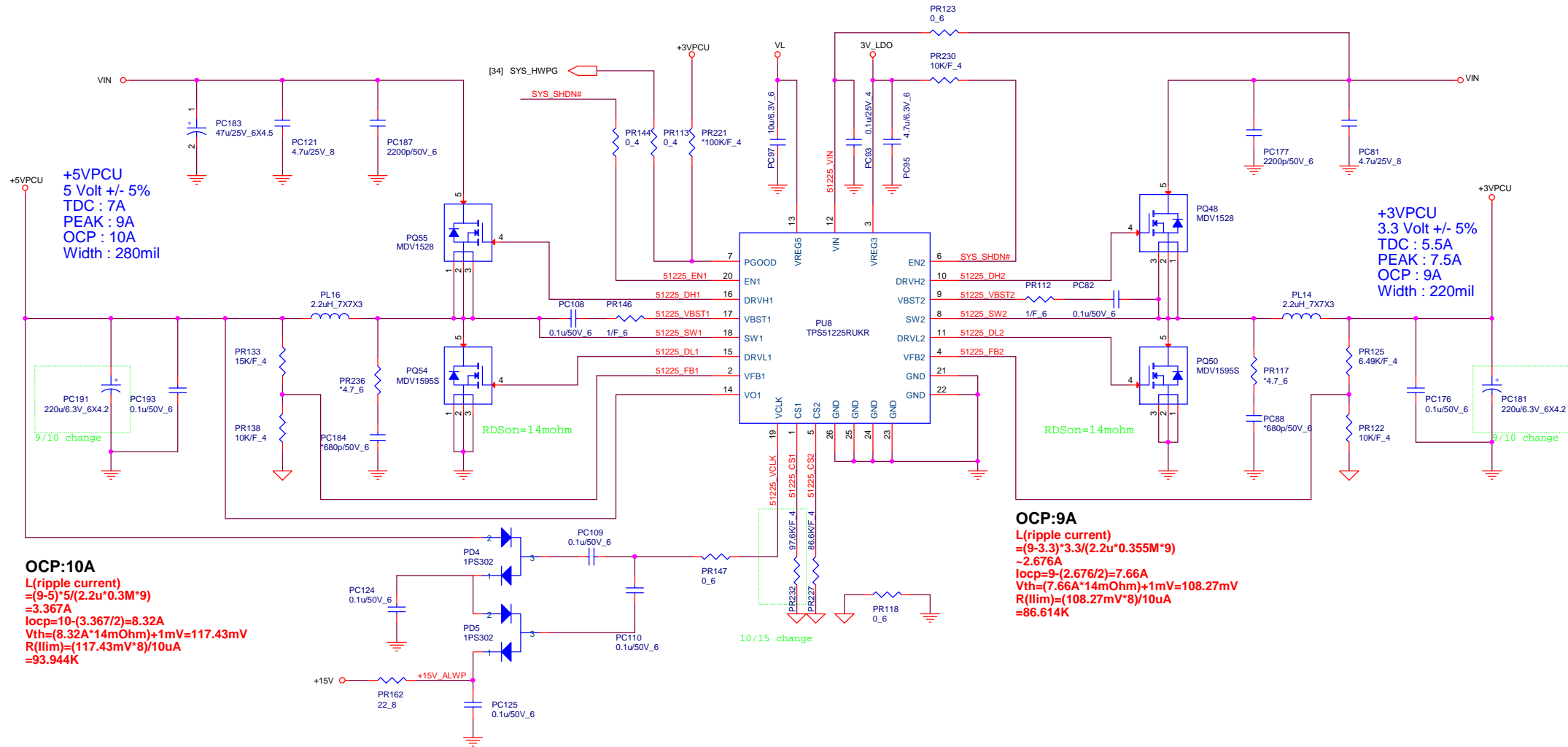


H.WPG(KBC)





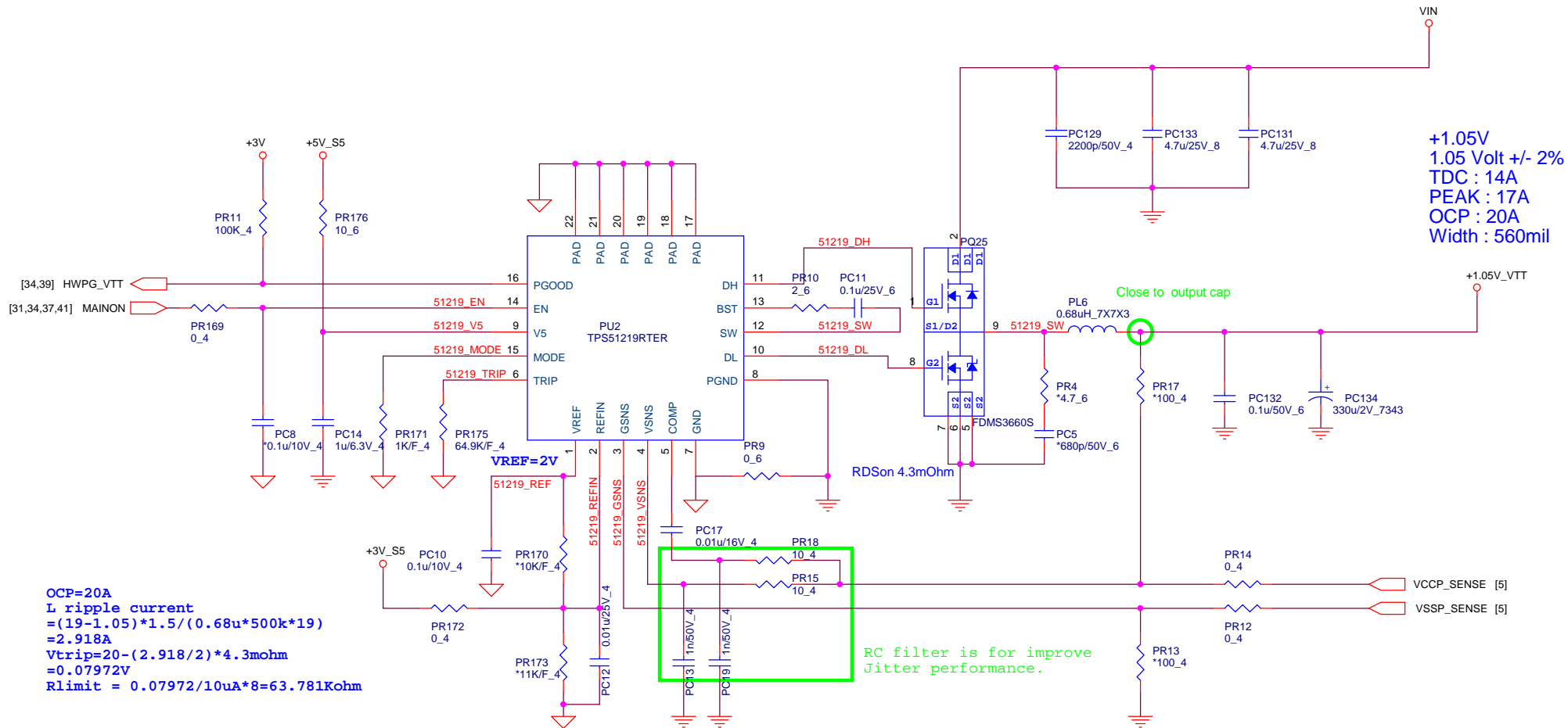
| | | |
|---|----------------------------|----------------|
|  Quanta Computer Inc. PROJECT : ZQK | | |
| Size | Document Number | Rev |
| | Charger(BQ24737RGR) | 1A |
| Date: | Monday, January 07, 2013 | Sheet 35 of 46 |





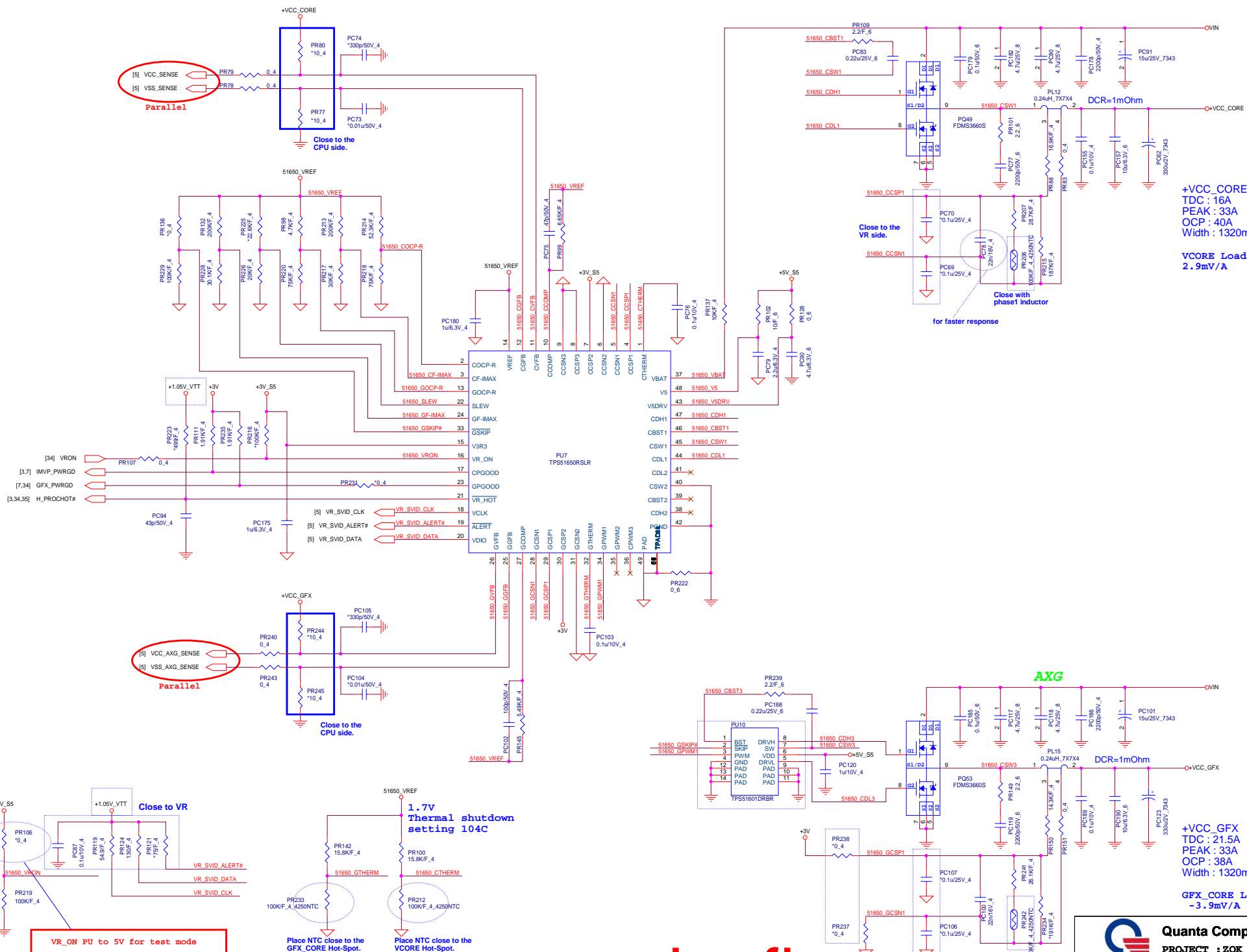
| | S3 | S5 | +1.5VSUS | REF | VTT |
|------------------|----|----|----------|-----|-----|
| S0 | 1 | 1 | ON | ON | ON |
| S3 (main on off) | 0 | 1 | ON | ON | OFF |
| S4/S5 | 0 | 0 | OFF | OFF | OFF |

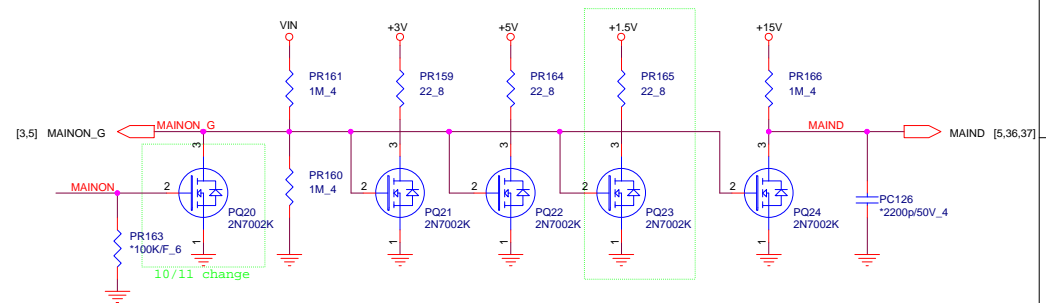
| | | |
|-------|--|------------------|
| Size | Document Number DDR 1.5V(TPS51216) | Rev 1A |
| Date: | Monday, January 07, 2013 | Sheet 37 of 46 |




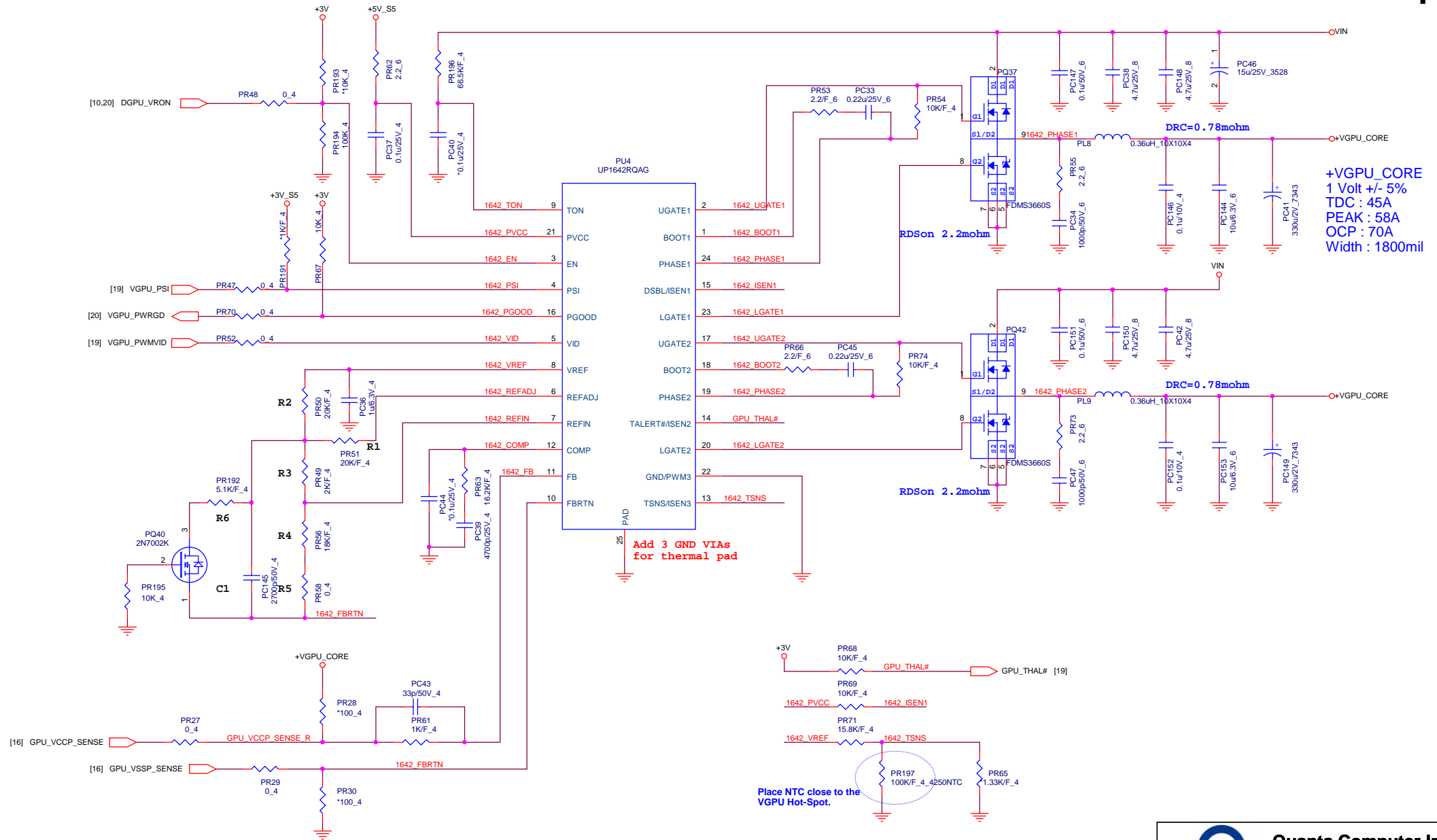
Quanta Computer Inc.
PROJECT : ZQK

| | | |
|-------|--------------------------|----------------|
| Size | Document Number | Rev |
| | +1.05V (TPS51219) | 1A |
| Date: | Monday, January 07, 2013 | Sheet 38 of 46 |






| | | | | |
|---|--------------------------|-------|----|-----------|
|  Quanta Computer Inc. PROJECT : ZQK | | | | Rev 1A |
| Size | Document Number | | | |
| +1.8V/Discharge/Thermal | | | | |
| Date: | Monday, January 07, 2013 | Sheet | 41 | of 46 |



Power Sequence

| | | | |
|---|--------------------------|---|----------|
|  | | Quanta Computer Inc. PROJECT : ZQK | |
| Size | Document Number | Rev 1A | |
| Power Sequence | | | |
| Date: | Monday, January 07, 2013 | Sheet | 44 of 46 |



| Model | Date | CHANGE LIST |
|-------|------|--|
| ZQK | 1203 | 1.Change C774 from 0.1uF to 39pF for ESD 2.Add C841~C850 39pF for ESD 3.Change U19,U21,U23,U26,U43,U46,U48,U49 PN from AKD5JGST404 to AKD5JGST407 |
| | 1205 | 1.Change LED1/LED2 PN : BEB00028ZA0 : FP : led19-123-y2st1d-c30-2t-4p 2.Change R383/R392 from 47 ohm to 56 ohm |
| | 1206 | 1.Change SW2 PN : DHPATE2CK03 : FP : sw-ate-2ck-v-tr-4p |
| | 1210 | 1.Delete PL2/PL3/PL4/PL5 2.Add RTC charge circiut and modify CN14 PN and FP (DFHS02FS032/ml1220-smt) 3.Update CN4 FP to "dp-adis0022-p001a-20p-smt" |
| | 1211 | 1.Add mSATA re-driver circuit 2.Change CN22 PN & FP as same as CN13 |
| | 1212 | 1.Modify Hole4 FP to H-TC197BC142D142P2 2.Change mSATA redriver power rail to +1.5V |
| | 1213 | 1.Add R828~R831 for co-layout 2.Add N14M-GE binary strap setting information |
| | 1214 | 1.Change USB DB power to 4 pins 2.Change CN4 PN to DFTD20FR001 |
| | 1217 | 1.Update Hole6/Hole17/Hole22 FP 2.Add C866 by FAE suggestion 3.Change C706 from 10uF to 4.7uF 4.Add pull down 100K by EC-Anda command (R832/R833/R834) 5.Change TEMP_MBAT fromPJ1 pin 5 to pin 6 (BATT_EN#) , then pin 6 is NC pin 6.Un stuff PR96 7.Add R835 and change R785 to 5.1M ohm 8.Mark R746 to NSW@ due to pin18 of U7 has internal +3V |
| | 1219 | 1.SUSLED# power from +3V_S5 to +3V_PCU (for Deep S3) 2.Change eDP connector CN8 PN and FP (DFHS40FS095 / gs12401-1011-40p-r-nh-smt) |
| | 1220 | 1.Add net PCH_SUSWARN# connect to Pin78 of EC (GPJ2) 2.Add net PCH_SUSACK# connect to Pin79 of EC (GPJ3) |
| | 1221 | 1.Change PR191 PU voltage from +3V to +3V_S5 |
| | 1224 | 1.Unstuff PR28/PR30 2.Reserve R837 |
| | 1225 | 1.Change PU4 PN from AL001642000 to AL001642001 |
| | 1226 | 1.Change U15 PN from AJ085870F03 to AJ085870F04 |
| | 1228 | 1.Co-layout mSATA re-driver IC-U51 (PS8521A & ASM1466) |
| | 0102 | 1.Unstuff PR191 (Already PU on HW side) 2.Reserve R842/R843 |
| | 0103 | 1.SWAP EC pin : BATLED1# change to pin32 ; ME_WR# change to pin25 |
| | 0104 | 1.Change U38 PN from AJ0QPRG0T03 to AJSLJ8C0T05 |
| | 0107 | 1.Update Hole6/Hole17 FP 2.Update Pad1 PN to FBZRK011010 3.Update Hole4 PN to FBAJ2005010 |

| | | | | | | | |
|--|--|---------|-----------------|-----|--------------|--|-----------|
|  Quanta Computer Inc. | | DOC NO. | PROJECT MODEL : | ZQK | APPROVED BY: | | DATE: |
| <small>File</small> | <small>Document Number</small> PROJECT : ZQK Change list | | PART NUMBER: | | DRAWN BY: | | REVISION: |
| <small>Date: Monday, January 07, 2013</small> | | | | | | | |

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